TECHNICAL MANUAL

OPERATOR'S, ORGANIZATIONAL DIRECT SUPPORT, GENERAL SUPPORT, AND DEPOT MAINTENANCE MANUAL

FOR

COUNTER, DIGITAL READOUT, ELECTRONIC ID-1341/GR AND INDICATOR, DIGITAL READOUT, ELECTRONIC ID-1342/GR

H E A D Q U A R T E R S , D E P A R T M E N T O F T H E A R M Y
J A N U A R Y 1 9 7 0

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 12 January 1970

TM 32-5820-207-15, 12 January 1970, is published for the use of all concerned.

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Chief of Staff.

Official:
KENNETH G. WICKHAM,
Major General, United States Army,
The Adjutant General.

WARNING

Be careful when working on the 115-volt ac line connections and the +330-volt dc circuits. Serious injury or death may result from contact with these terminals.

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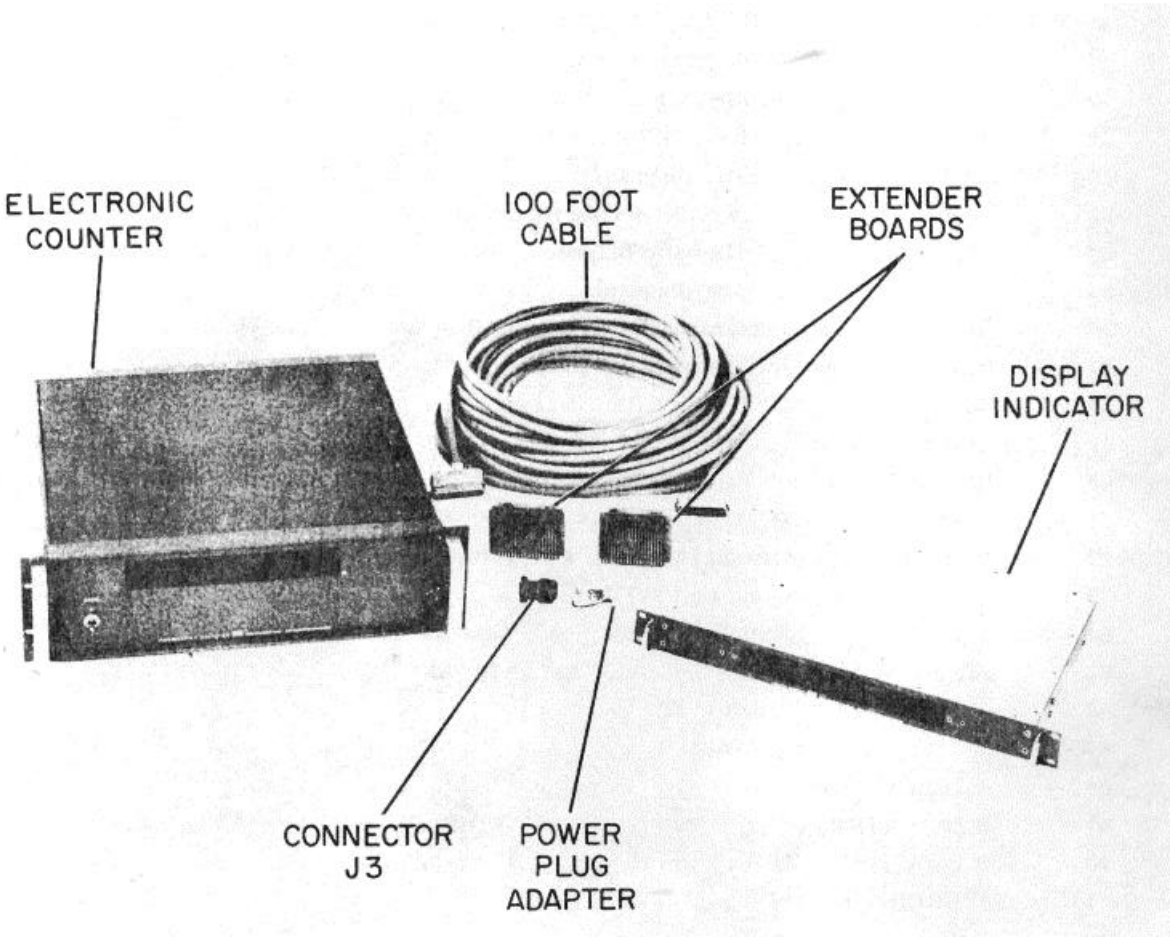


Figure 1. Electronic Counter, Major Units.

CHAPTER 1

INTRODUCTION

SECTION I. GENERAL

1. Scope

This manual describes the Counter, Electronic, Digital Readout ID-1341/GR (hereafter called electronic counter)and Indicator, Digital Display, Electronic ID-1342/GR(hereafter called display indicator). (See fig. 1.) Instructions are given for installation, operation, theory, and maintenance. The manual also includes operation under usual conditions, cleaning and inspection, replacement of parts, troubleshooting, calibration, and repair applicable to all categories of maintenance.

2. Forms and Records

a. Report of Damaged or Improper Shipment. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment) as prescribed in AR 700-58.

b. Equipment Records. Equipment records will be maintenance in accordance with TM 38-750. Equipment Improvement Reports will be forwarded to: Commanding Office, USASA Material Support Command, ATTN: IAMME/M, Vint Hill Farms Station, Warrenton, Virginia, 22186.

c. Parts List Form. Fill out and forward DA Form 2028, Recommended Changes to Technical Manuals Parts Lists or Supply Manuals 7, 8, and 9, directly to: Commanding Officer, USASA Material Support Command, ATTN: IAMME/M, Vint Hill Farms Station, Warrenton, Virginia, 22186.

d. Comments on Manual. Forward all other comments concerning the publication direct to: Commanding Officer, USASA Material Support Command, ATTN: IAMME/M, Vint Hill Farms Station, Warrenton, Virginia, 22186.

Section II. DESCRIPTION AND DATA

3. Purpose and Use

a. The electronic counter is a rack mountable instrument designed to automatically track and display a receiver's tuning over a 1 KHz to 2.5 KHz frequency range in five overlapping bands. Direct readout of the receiver frequency is achieved by measuring the receiver local oscillator frequency and presetting the readout counters to subtract the radio receiver intermediate frequency. (See fig. 2.)

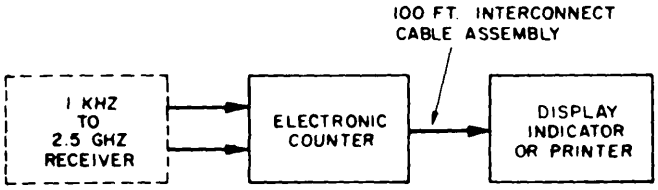


Figure 2. Electronic Counter Use, Block Diagram.

b. The instrument is used only with radio receivers which the local oscillator tracks above the receiver input frequency. Two fixed offset frequency compensations for 21.40 MHz and 60.0, MHz intermediate frequencies are installed in the instrument. Provision is also made for one additional offset frequency which may be installed. Input band frequency and intermediate frequency compensation switching is automatically accomplished by remote programming signals supplied by the radio receiver.

c. A display indicator may be used with the electronic counter to permit monitoring the frequency display up to 100-feet away from the receiver. All the necessary power and the readout control function requirements are supplied through the 100-feet interconnection cable.

4. Electronic Counter Technical Characteristics

Frequency Ranges:

Input:

Band I	.001 to 121.4 MHz
Band II	81.4 to 321.4 MHz
Band III	295 to 560 MHz
Band IV	550 to 1060 MHz
Band V	1.0 GHz to 2.5 GHz

Offset:

Band I and II	21.4 MHz
Band III and IV	60 MHz
Band V	Optional

Resolution:

All Bands:	1 KHz
Accuracy:	±1 KHz ± oscillator stability

Oscillator Stability:

Short term	5×10^{-8}/day average;
Long term.	3×10^{-7}/week after 24 hours;
Temperature	$\pm 5 \times 10^{-9}$/°C(-20°C to + 60°C).

IF Offset Compensation

(L.O.set above received freq.)

Fixed:	21.4 MHz (reset to 9978.600 MHz) 60 MHz (reset to 9940.000 MHz)
Optional:	Provision is made for one additional offset.
	Input Channel:
Sensitivity:	30 mv rms into 50 ohms (-17.5 dbm, 0.018 mw) from 1 KHz to 1.06 GHz decreasing to 50 mv rms into 50 ohms (-13 dbm, 0.05 mw) at 2.16 GHz
Amplitude:	To 0.5V rms into 50 ohms (7 dbm, 50 mw).
Impedance:.	50 ohms, 1.5:1 maximum VSWR.
External Standard Input:	1 MHz; 1V rms into 1000 ohms.
Time Reference Output:	1 MHz, 1 v rms nominal from 1000 ohms source impendance; Type BNC female, rear panel.

Remote Programming:

Function	Performs band, IF offset, and input connector switching.
Input	+12 to +24 vdc at 10ma max. To one of five pins on a rear panel connector. Each pin relates to one of the five conditions given in the "Input Frequency Range" table.
Connector	Type MS3112A14-19P, rear panel; MS3116B14-19S mating connector supplied.
Reset	Automatic at a nominal rate of approximately 0.25 seconds.

Print Output:

Function	To provide readout information and power needs to the Display Indicator
Printout Code	8-4-2-1 negative true negative level BCD ("0"=-0.3 volts nominal, "1"=-9 volts nominal for all seven digits; 6,800 ohm source impedance.
Print Command	Automatic positive going step at end of count cycle, -4 volt to +4 volt; 15,000 ohm impedance
Connector::	Amphenol 57-40500, rear panel
Visual Readout:	Seven digit in-line, long life glow tubes; fixed decimal point reading in Mc; window filter and RF screening; stored presentation only.

Environment:

Temperature:	Operating, 0°C to 60°C. Storage, -35°C to 75°C.
RFI	Per MIL-1-26000, Class III.
Moisture/Fungus:	Per MIL-E-4158C.
Power:	115-volts AC± 10%, 48-62 Hertz, 105 watts (plus 15 watts crystal oven power).

5. Display Indicator Technical Characteristics

Input:	Seven digit, 8-2-4-1 negative true negative level BCD ("0"=-0.3 volts nominal, "1"=-9 volts nominal.

Environment:

Temperature	Operating, 0°C to 60°C. Storage, -35°C to 75°C.
RFI:	Per MIL-126000, Class.

Moisture/Fungus ..... Per MIL-E-4158C
Power: ..... Derived from the Electronic Counter

6. Components of Display Indicator

The components shipped with the equipment are as follows:

Quantity	Item	Dimensions (in.)			Unit Weight (lb)	Figure No.
		Height	Depth	Width		
1	Electronic Counter	5-1/4	17-1/4	19	38	1
1	Display Indicator	1-3/4	12	19	5	1
1	100 feet Interconnect Cable Assembly	-	-	-	14	1
2	PC Board Extenders	-	-	-	1/4	1
1	AC Line Ground Adapter	-	-	-	1/4	1
1	Cable Connector	-	-	-	1/4	1

7. Description of Electronic Counter

a. The electronic counter is an all solid state frequency counter designed to automatically track and display receiver tuning over a 1 KHz to 2.5 GHz frequency range. Direct readout of the receiver frequency is accomplished by measuring the receiver's local oscillator output frequency and automatically subtracting the receiver's intermediate frequency difference. The electronic counter with receivers which are designed with local oscillator frequencies that track higher than the receiver input radio frequency.

b. The electronic counter operates over five frequency bands and provides fixed offset compensation for the intermediate frequencies of 21.40 MHz and 60.0 MHz. An additional offset compensation capability (not included) and a remote display indicator may be used with the electronic counter. All the necessary signals are supplied to the remote display indicator (in a parallel binary coded decimal format) through a 100-feet interconnecting cable assembly.

c. The electronic counter is connected to the receiver and automatic operation is initiated when power is applied by the POWER switch. Automatic frequency band and intermediate frequency offset compensation switching is supplied to the electronic counter as the radio receiver bands are selected. All circuit functions are automatic and the numerical readout rapidly displays the correct frequency measurement to which the receiver is tuned. While the receiver is being tuned or if a noise signal is present, the fixed offset measurement error will be displayed.

Note: The electronic counter can be used as a direct reading frequency counter with no IF offset. Instructions for using the electronic counter in this manner are given in paragraph 14a (2).

d. Frequency tracking from 1 KHz to 2.5 GHz is displayed on a seven digit in-line glow-tube, numerical indicator which is automatically reset (cleared at a recycle rate of 250 milliseconds nominal). A parity check circuit (error detector) automatically detects measurement errors or permits the correct frequency to be displayed if no errors exist.

e. The time base generator reference is a one-megahertz, temperature stabilized crystal oscillator. The onemegahertz crystal provides the master clock reference for all frequency measurements. The crystal oven heating element is connected to the power input cable (by passing the POWER switch) to assure long-term stability of the crystal frequency in normal operation.

8. Description of Display Indicator

a. The display indicator is a separate unit containing a numerical seven digit display indicator of in-line glowtubes and is used in conjunction with the electronic counter. The unit provides remote frequency readout indications and is slaved to the electronic counter readout circuits through a 100-feet interconnect cable assembly. Any change in the frequency display is also transmitted to the display indicator readout.

b. Remote mechanical printer capabilities are available at the electronic counter PRINT-OUT connector (J4) although a second interconnect cable assembly is required.

Note: This unit is wired for negative 13CD output logic. The levels are as follows:

Code 8-4-2-1 BCD, binary "0" -0.3 volts, binary "1" -9 volts, 6.8K ohm source impedance.

The printout connector, code levels and print command are compatible with the HP model 562A digital printer equipped with 7 of the option 23 column boards and option 30 BCD input connector assembly.

CHAPTER 2

INSTALLATION

Section I. SERVICE UPON RECEIPT OF EQUIPMENT

9. Unpacking

The electronic counter is shipped in a specially constructed container to provide maximum protection to the equipment (luring transit. Use care when unpacking to prevent damage to the equipment, such as the cabinet paint finish, controls. indicator, connectors, etc.

a. Packaging Data. packed for shipment, the units of the electronic counter are placed in a carton and packed in a corrugated shipping box. A typical shipping box and its contents are shown in figure 3 and 4. The dimensions, volume, and contents of the shipping boxes are listed in table 1.

Table 1. Packaging Data

Box No.	Contents	Dimensions (in.)	Volume (cu ft.)	Weight (lb)
1 of 2	Electronic Counter	9 x 24-1/2 x 24-1/2	29	50
2 of 2	Display Indicator	5 x 27 x 24	15.75	30

b.. Removing Contents.

(1) Cut and fold back the outer carton end flaps.

(2) Remove the envelopes that contain the manuals and accessory parts.

(3) Remove the equipment in the dust protection bag from the inner carton.

(4) Remove the equipment in the dust protection bag from the inner carton.

(5) Open dust protection bag and remove equipment.

10. Checking Unpacked Equipment

a. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, report the damage on DD Form 6 (para 1-2).

b. See that the equipment is completed as listed on the packing slip. Report all discrepancies in accordance with TM-38-750 for shortage of a minor assembly or part that does not affect proper functioning of the equipment.

c. If the equipment has been used or reconditioned, see whether it has been changed by a modification work order (MWO). If the equipment has been modified, the MWO number will appear on the front panel near the nomenclature plate. If modified, see that any operation instruction changes resulting from the modification have been entered in the equipment manual.

Note: Current IMWO'S applicable to the equipment are listed in USASA Circular 310-11 (C).

11. Placement of Equipment

a. The electronic counter front panel permits mounting in any equipment rack provided the general environment is within the limits of the equipment as specified in Chapter 1, Section II. The mounting rack should be firm and free from vibration. Total weight of individual units is listed in table 1.

b. Since the units are fixed rack mounted, any repair work will require the removal of the units from the rack to a workbench area. Access to the electronic counter rear panel controls must be provided.

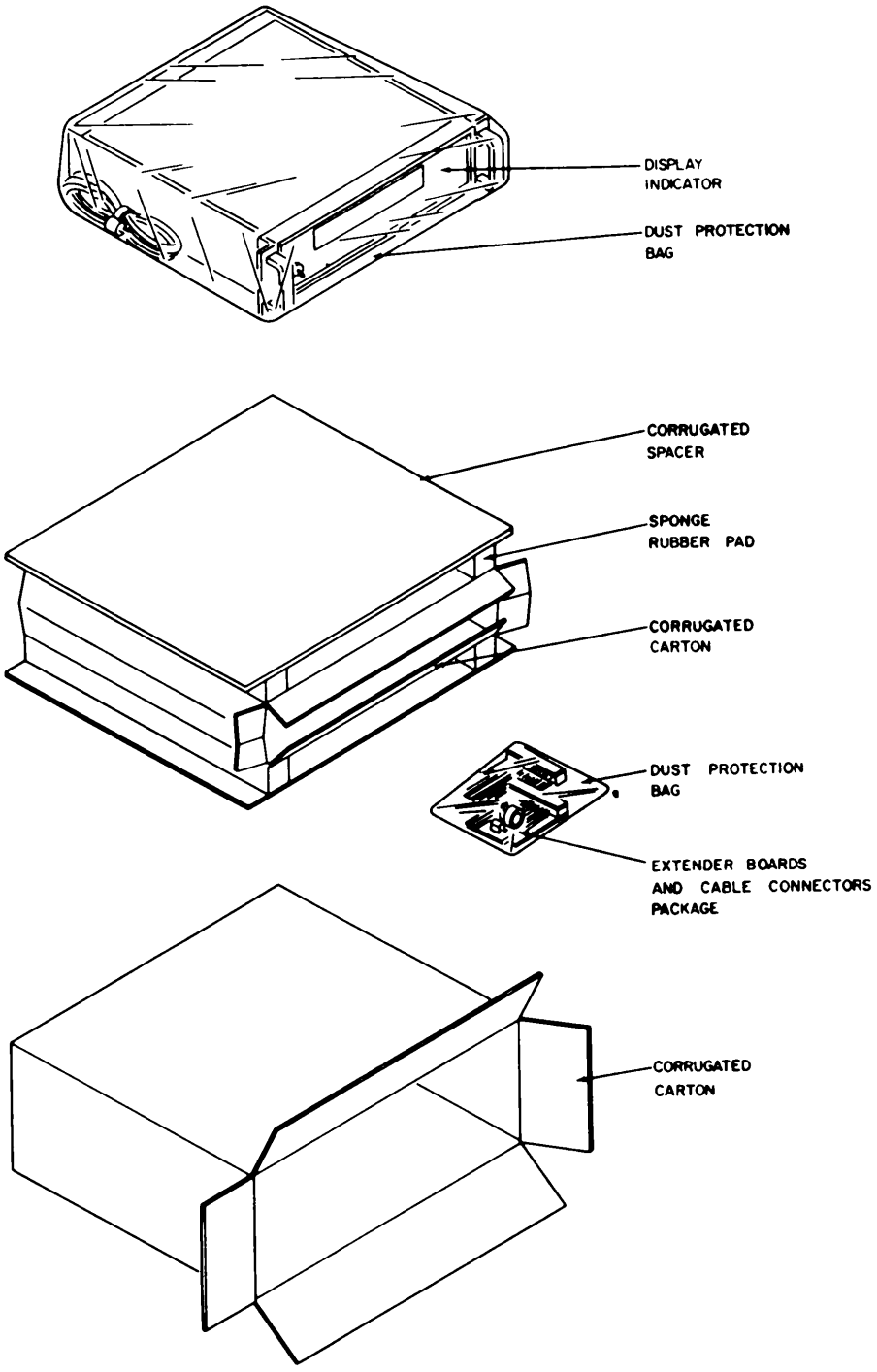


Figure 3. Electronic Counter Packaging.

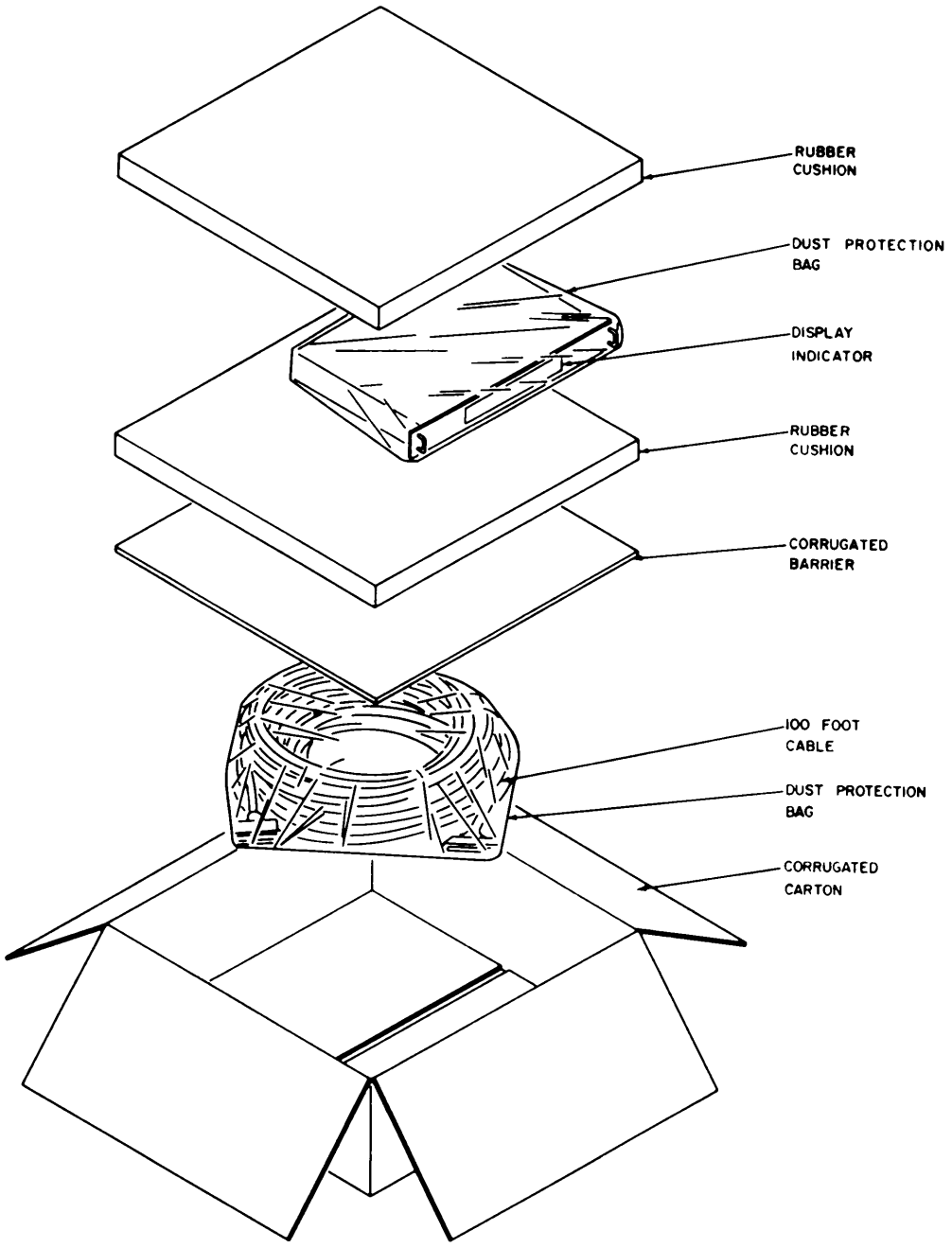


Figure 4. Display Indicator Packaging.

12. Tools and Test Equipment Required for Installation

No special tools or test equipment are required for installation.

13. Installation of Equipment

a. Electronic Counter, Rack Mounting. The electronic counter is ready for rack mounting after unpacking is completed. No additional assembly is required. To install the electronic counter in a rack assembly, proceed as follows:

(1) Remove a blank panel in the rack where the electronic counter is to be mounted. Retain mounting hardware.

(2) Install the display indicator in the rack space previously occupied by the blank panel. Secure with four mounting screws previously removed.

(3) Install cable connections as detailed in paragraph 14.

b. Display Indicator, Rack Mounting. The Display Indicator is ready for rack mounting after unpacking is completed. No additional assembling is required. To install the display indicator in a rack assembly, proceed as follows:

(1) Remove a blank panel in the rack where the display indicator is to be mounted. Retain mounting hardware.

(2) Install the display indicator in the rack space previously occupied by the blank panel. Secure with four mounting screws previously removed.

(3) Install the interconnection cable assembly between J22 on the display indicator rear panel and J4 on the electronic counter rear panel.

14. Equipment Cabling

The electronic counter is shipped ready for use except for signal input cabling (see fig. 5). Since these cables are normally a part of the installation rack internal cabling, they are not included with the equipment.

Caution:

The display indicator interconnect cable assembly is not interchangeable with a mechanical printer interconnect cable.

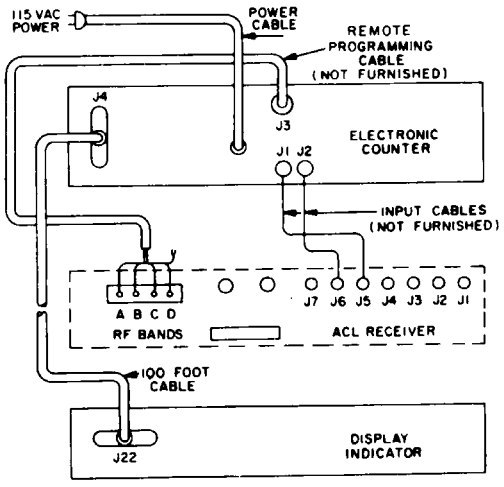


Figure 5. Electric Counter, Cable Connections.

a. Receiver Programming Cable Connections

(1) Connections for Normal Operation. The electronic counter is shipped without a receiver programming cable. A five or six conductor cable (as required by the radio receiver used) must be constructed using the cable connector supplied with the electronic counter. Although the electronic counter. Although the electronic counter is not supplied with Band No. V capabilities, the wire may be installed (but not connected) for future use. Refer to the following list for the applicable pin connections for the receiver frequency band used.

From Connector 57-4050 Pin No.	To Receiver Band No.	Wire Size
K	I	16 AWG
L	II	16 AWG
M	III	16 AWG
N	IV	16 AWG
P	V	16 AWG
G	Chassis Grd.	16 A'WG
V	+12 Volts	

(2) Connections for No IF Offset. To use the electronic counter with No IF offset, remove preset generator circuits A22 and A23. Then wire programming cable connector A49J5 as follows:

(a) For band I operation, connect jumper wire between pins V and K.
(b) For band II operation, connect jumper wire between pins V and L..
(c) For band III operation, connect jumper wire between pins V and M.
(d) For bind IV operation, connect jumper wire between pins V and N.

b. Receiver Signal Input Cables. Input signals are supplied to the electronic counter through two radio frequency coaxial cables connected to the radio receiver output jacks. Two lengths of RG58/U coaxial cable with a BNC connector on one end and type N connector on other are required. Connect one cable between J1 on the electronic counter an(d the receivers 1 KHz to 300 MHz output jack. Connect the second cable between J2 and the receivers : oo00 MHz to '2.5 GHz output jack. Cable lengths will be as required for the individual installation.

c. Print-Out Cables. The electronic counter may be used with a mechanical printer (Hewlett Packard Co., Model 562A) instead of the display indicator if desired. The binary -coded-decimal output signals are available at PRINT-OUT connector J4. The use of a mechanical printer will require the fabrication of a new interconnection cable. Cable length will be as required for the individual installation but must not exceed 100 feet. Refer to Table 2 for connector pin wiring of the cable used between the electronic counter and a mechanical printer. Refer to Table 3 for cable wiring between the electronic counter and the display indicator.

Note: Because of probable noise interference the 100-foot cable should be of the same type used with the display indicator. The cable used is Eldorado Electronics Part Number 11--4175.

d. Power Cable. The electronic counter is equipped with a three-wire power cable. After the instrument is installed in an equipment rack, and the programming and the signal input cables are connected, connect the power cable to any convenient ac power outlet. The exposed portions of the instrument are grounded for safety.

When only a two-blade outlet is available. use the power cable adapter supplied with the display indicator.

Connect the short wire from the side of the adapter to a convenient grounding point.

Note: Use of three-wire ground power cable does not eliminate the USASA requirement for a separate grounding strap from equipment to the rack ground bus.

Table 2. Mechanical Printer Cable Wire List

PIN NO.	COLOR	FUNCTION	PIN NO.	COLOR	FUNCTION
1	Brown	10^0 #1	26	Yellow	10^0 #4
2	Red	10^0 #2	27	Gray	10^0 #8
3	Brown	10^1 #1	28	Yellow	10^1 #4
4	Red	10^1 #2	29	Gray	10^1 #8
5	Brown	10^2 #1	30	Yellow	10^2 #4
6	Red	10^2# 2	31	Gray	10^2 #8
7	Brown	10^3 #1	32	Yellow	10^3 #4
8	Red	10^3 #2	33	Gray	10^3 #8
9	Brown	10^4 #1	34	Yellow	10^4 #4
10	Red	10^4 #2	35	Gray	10^4 #8
11	Brown	10^5 #1	36	Yellow	10^5 #4
12	Red	10^5 #2	37	Gray	10^5 #8
13	Brown	10^6 #1	38	Yellow	10^6 #4
14	Red	10^6 #2	39	Open	10^6 #8
15	Open	Open	40	Open	Open
16	Open	Open	41	Open	Open
17	Open	Open	42	Open	Open
18	Open	Open	43	Open	Open
19	Brn/Blk	Dec. Pt. NC	44	Yel/Blk	Dec. Pt. NC
20	Wh/Grn	Dec. Pt. NC	45	Grn/Blk	Dec. Pt. NC
21	Wh/Blk	Read	46	Red/Blk	+300
22	Wh/Red	+ 12	47	Wh/Blue	-12
23	Wh/Org	+ PC	48	Wh/Vio	-PC
24	Wh/Yel	-Ref-(-12v)	49	Wh/Gry	Scan NC
25	Blk (24ga)	Ground	50	Blk (24 ga)	Ground

Notes

NC Wire is installed, but tied off at open end

Open No wire installed

PC Signifies Print Command

Table 3. Display Indicator 100-Foot Cable Wire List.

PIN NO.	COLOR	PIN NO.	COLOR
1	Black	27	Wh/Brn
2	Blk/Brn	28	Wh/Red
3	Blk/Red	29	Wh/Org
4	Blk/Yel	30	Wh/Yel
5	Blk/Grn	31	Wh/Grn
6	Blk/Blu	32	Wh/Blu
7	Blk/Vio	33	Wh/Vio
8	Blk/Grey	34	Wh/Grey
9	Blk/Wh	35	White
10	Vio/Blk	36	Red/Org
11	Vio/Org	37	Red/Yel
12	Vio/Yel	38	Red/Grn
13	Vio/Blu	39	Red/Blu
14	Violet	40	Open
15	Open	41	Open
16	Open	42	Open
17	Open	43	Open
18	Open	44	Open
19	Open	45	Open
20	Open	46	Red/Vio
21	Red	47	White #24 wire
22	Red/Blk & Red/Wh		4 # 18 wires 3 Blue
23	Open		1 Green
24	Open	48	Open
25/50	4 # 18 wires 3 Brown	49	Open
	1 Orange		
26	Wh/Blk		

Note: Open indicates no wire is installed

Section II. INITIAL ADJUSTMENTS OF EQUIPMENT

15. Extent of Initial Adjustments

The electronic counter is fully automatic during operation. All controls required for operation are mounted on the front and rear panels. No additional adjustment of controls is required.

16. Initial Adjustments

Check that the 1-MHz oscillator EXT-INTERNAL switch, located on the rear panel, is set at the INT position.

CHAPTER 3

OPERATING INSTRUCTIONS

Section I. OPERATOR'S CONTROL AND INDICATORS

Note:
This section covers only items used by the operator. Items used by maintenance personnel are covered in instructions for the appropriate maintenance echelon.

17. General

The electronic counter is fully automatic during operation. Only power application by the front panel power switch is required to operate the equipment.

18. Operating Controls and Indicators

The electronic counter front panel operating control and indicator is shown in figure 6. The display indicator is shown in figure 7. The control name and function is listed in table 4.

Table 4. Electronic Counter Operating Control and Indicator

Control or Indicator	Function
POWER switch	In the ON position, turns on the electronic counter.
XXXX, XXX Mc	Readout Display. Provides a numerical display in megacycles of the frequency measured.

19. Measurement Error Indication

During normal operation a measurement error indication may occur. Normally, the electronic counter will display the frequency that is being monitored. Since this frequency will be in the frequency range to which the radio receiver is being tuned (as indicated by the tuning indicator) dissimilar frequency indications will be obvious. However, if a measurement error occurs (e.g., due to a malfunctioning receiver) a parity consistency check circuit will detect such errors and cause the electronic counter to display a frequency that will be equal to the preset number (9978.600 Bands I and II and 9940.000 Bands III and IV).

Note
Any continuous or erratic measurement error indications should be investigated to determine if the equipment is functioning properly.

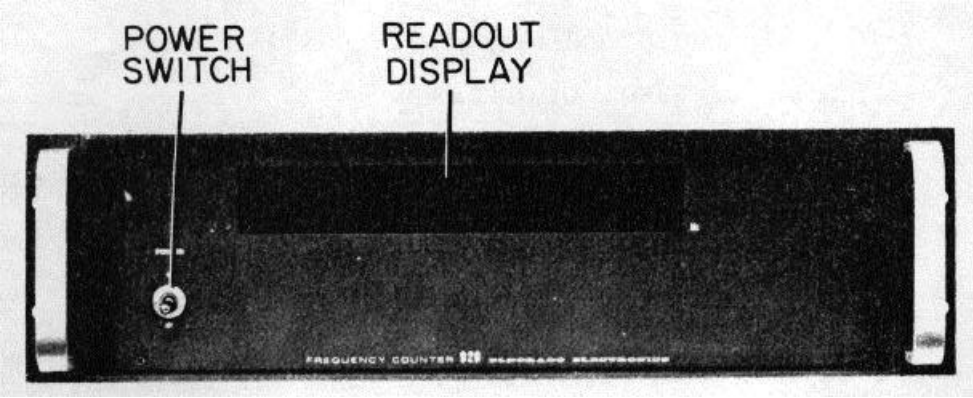


Figure 6. Electronic Counter, Controls and Indicators

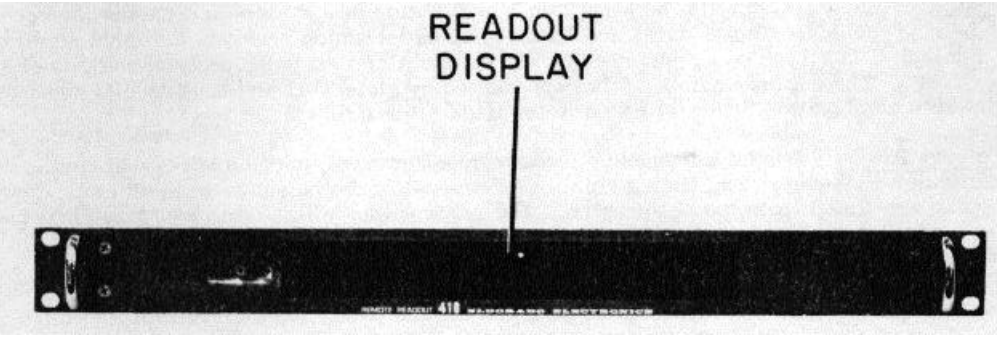


Figure 7. Display Indicator, Controls and Indicators

CHAPTER 4

THEORY OF OPERATION

Section I. GENERAL

20. Scope

a. This chapter contains the theory of operation for the electronic counter circuits. Included are the simplified block diagram description, an overall block diagram description, and detailed block diagram level descriptions of the individual printed circuit boards.

b. Section I defines terminology used. Also contained in Section I are typical basic circuit descriptions and pulse function identifications used in the electronic counter and display indicator circuits.

21. Terminology and Pulse Identification The following definitions of terms are used throughout the manual.

a. Counters

(1) Binary. A bistable multivibrator (flip-flop) used to divide or store binary information.

(2) Decimal Weight. Numerical value assigned to the output of each binary. In a 1248 code, decimal weights are assigned as follows: A binary, 1; 13 binary, 2; C binary, 4; D binary, 8.

(3) 1 State. One of a pair of transistors in a binary conducting. Output of binary indicates decimal weight present.

(4) 0 State. Opposite transistor in a binary conducting. Output of binary indicates decimal weight absent.

(5) Binary-Coded-Decimal. Binary-coded-decimal (BCD) information is coded in such a way that each decimal digit may be represented by a unique combination of 1 and 0 states of four binaries.

(6) Truth Table. A table which lists the allowable 1 or 0 states of a system of binaries for each decimal digit to be represented. These states are listed in an order which presents the most significant digit first. Example: In a 1248 code, binaries D, C, B, and A are assigned decimal weights of 8, 4, 2, and 1 respectively. The decimal number 5 is represented by state 0101 and weights of 4 and 1 are present. The allowable combination (0101) is listed in the truth table (table 5).

b. Timing and Signal Pulses. During a frequency measurement interval, there are several timing operations which occur in a particular sequence. The timing relation of several of the pulses to each other is shown in Figure 8. All the pulse are timed from the reset pulse. The reset pulse, which occurs at a nominal recycle interval of 250 milliseconds, controls the timing generator to start the sequence of events.

(1) Reset Pulse. The reset pulse serves to clear all circuits; that is, sets the counter and divider circuits to a normal state and sets the ratio and control circuit and parity logic circuits for a counting interval. The trailing edge of the reset pulses serves to trigger the preset generator circuits.

(2) Preset Pulse. The preset pulse is developed by the preset generator circuits and serves to set preselected flip-flops in the decade counters to specific states.

(3) F-Frequency. The f-frequency is the unknown input frequency that will be measured.

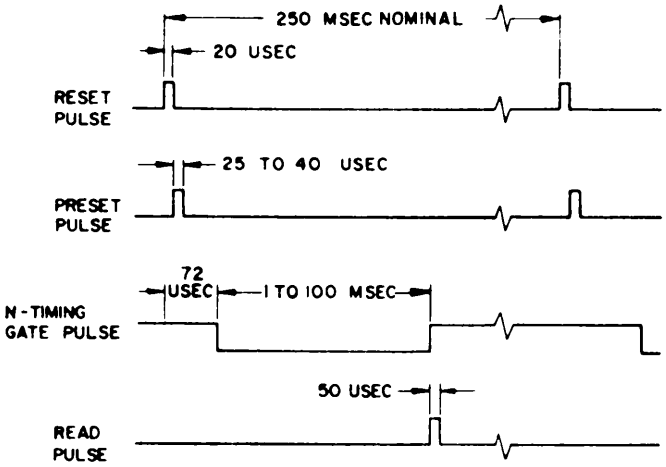


Figure 8. Electronic Counter Timing Functions.

Table 5. Decade Counting Unit Truth Table

D	C	B	A	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	10=0

(4) F/N Frequency. The f/N frequency is the output frequency developed by the I.C. and S.C. circuits.

(5) F_2 Frequency. The f_2 frequency is a 1.5 KHz frequency generated in the F.S. circuit and serves as the slow time base signal.

(6) F_2N Frequency. The f_2N frequency is a function of frequency f applied to the I.S. circuit and the output from the F.S. circuit.

(7) Four-N-Frequency. The 4N frequency is a burst of N developed in the ratio gate circuit from the ratio gate circuit from the ratio gate pulse and the f_2N signal.

(8) N-Ratio Level. The N-Ratio level is a voltage applied to the I.C circuit and serves to set the f/N signal ratio level.

(9) Ratio Gate Pulse. The ratio gate pulse applied to the ratio gate circuit serves to extract the N-signal from the4 f_2N signal to develop the 4N signal. The time of the 4N bursts is equal to $\frac{f2/^8}{2}$

(10) Bursts of N Pulses. The bursts-of-N output pulses is developed from the 4N pulse train thru the "B" logic.

(11) One-Megahertz Clock Frequency. The 1 MHz clock frequency is a reference source for all timing functions.

(12) Read Pulse. The read pulse serves as an enabling pulse to transfer to the memory and readout circuit the N-Count data totalized in the decade counters.

(13) Display Pulse. The display pulse, generate as a function of the stop flip-flop being set (N-Timing gate off-going time) provides an enabling pulse to the read one-shot flip-flop. Also when the display pulse is gated the error reset pulse in the A.D. circuit triggers the divide-by16 circuit.

(14) Error Reset Pulse. The error reset pulse triggers the reset circuit and causes a reset pulse to be generated when a consistancy error is detected. After three (3) error resets the N-Ratio level will change.

(15) Alternate Reset Pulse. The alternate reset pulse resets the B logic circuit after a consistancy error check is completed

(16) Nine-Carry Pulse. The nine-carry pulse is developed in the time base counter. It occurs only when all decades reach a count of nine (9). This coincidence is used to trigger open and shut the N-Timing gate.

(17) Odd-Even Pulse. The odd-even pulse gated with the parity enable pulse output, provides a trigger pulse to the error reset flip-flop if the B logic circuit final binary fails to reset to a reset state after two bursts-of-N.

(18) A Reset Pulse. The A reset pulse resets the A logic circuit after a frequency measurement is made to assure the alternate reset flip-flop is reset.

(19) N-Timing Gate. The N-Timing gate pulse controls the counting time of the C.U. circuit. The pulse is developed in the ratio and control circuit.

22. Typical Basic Circuits

The following paragraphs describe basic circuits used in the electronic counter. Although the instrument is comprised of a number of individual printed circuit boards and associated wiring, its operation may be best understood by understanding the operation of the types of circuits used.

a. The Diode. Semiconductor diodes are used in signal-handling circuits and in power supply rectifier and regulator circuits.

b. The OR Gate. Two or more diodes are sometimes used as an OR gate. The OR gate is a multiple-input circuit which requires only one input to produce a true output condition. Figure 9 shows some OR gate configurations.

c. The AND Gate. The AND gate (or coincidence circuit) is a multiple-input circuit which requires the presence of all input signals to produce a true output condition. Figure 9B shows an AND gate configuration in which -an input signal is passed only when properly polarized control voltages are applied..

d. The Inhibit Gate. An inhibit gate normally passes a signal. Adding a second signal closes the gate and prevents the signal from going through. One of the most common forms of the inhibit gate is the series gate shown in figure 9C. If the diode is biased off, the gate is closed, and pulses do not reach the output. When the diode is biased on, the pulses pass through the gate and reach the output.

e. Limiter or Clipper. The limiter or clipper is a circuit which removes positive or negative peaks of waveforms. It can be used either as a waveform shaping circuit, or as a protective device to prevent excessive voltages from reaching a sensitive circuit. Figure 9D shows a limiter which prevents the negative peak or a pulse from going more negative than about -0.6 volt. Note that for a conducting silicon diode the cathode voltage is about 0.6 to 0.8 volt more negative than the anode.

f. Clamper or Dc Restorer. The clamper or dc restorer is a circuit which establishes either the positive or negative peak of a waveform at a particular dc reference voltage. This provides a definite base line voltage for the waveform. Figure 9E shows a clamper which provides a baseline of about +5 volts for a negative pulse.

g. Regulator. A diode regulator uses either the constant reverse-bias breakdown voltage characteristic of a breakdown diode or the (constant forward-bias voltage drop characteristic of a semiconductor diode. Power supply reference voltages are generally provided)by breakdown diodes which' maintain a constant voltage when supplied with a reverse-bias voltage greater than their specified breakdown voltage. Regulated voltages can also be provided by a forward-biased diode which maintains a constant volt drop. Figure 9F shows connections for both types of diodes.

h. The Transistor. Transistors are used throughout the display indicator in circuit configurations such as the amplifier, the flip-flop or binary, the trigger circuit, and the one-shot multivibrator. In the following paragraphs, basic transistor operation and a few basic transistor circuits are discussed. These paragraphs discuss the easily observed changes in currents and voltages in transistor circuits which help technicians locate circuit faults but do not attempt to describe how transistors work internally.

i. Biasing and Conduction. Vacuum tubes and transistors are functionally similar. In the tube a small grid-to-cathode voltage controls a larger plate-to-cathode current flow. In a transistor a small base-to-emitter current controls a large collector-to-emitter current. A comparison of basic vacuum tube, NPN transistor operation is shown in figure 10A. Indicated current represents conventional flow of positive charges external to the transistor and is not intended to indicate flow of carriers inside the transistor structure. Notice that the effect of emitter-base-collector voltages is totally reversed between NPN and PNP transistors.

j. Amplifiers. As with vacuum tubes, three basic amplifier types are available (fig. 10B). These amplifiers may be used alone or in combination to form complex circuits.

k. Flip-Flop. The flip-flop is ;bi-stable two-transistor circuit in which one transistor conducts, holding the other cut off. Each input pulse causes a reversal of states; that is, the cut off transistor is turned on and the conducting transistor is cut off.

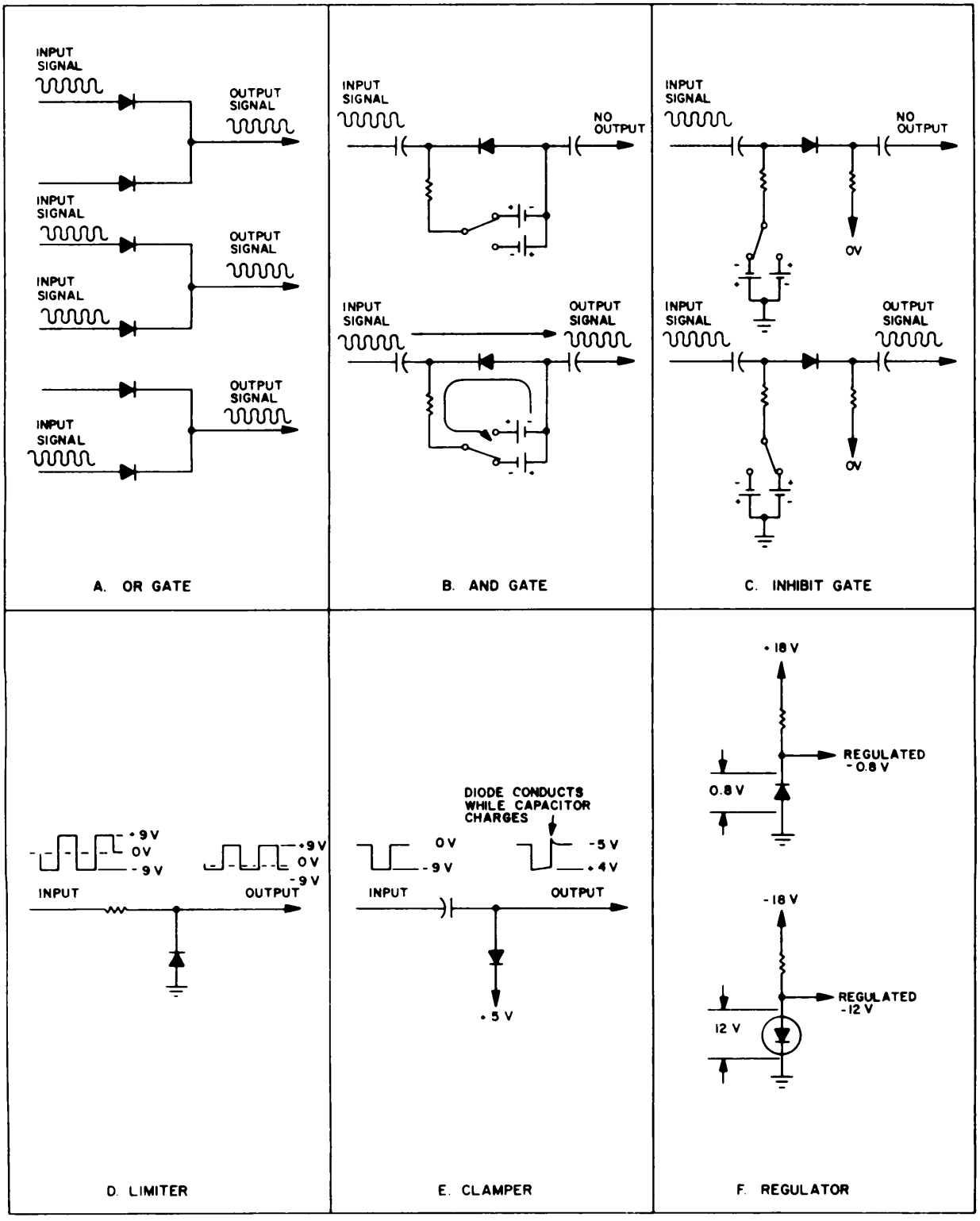
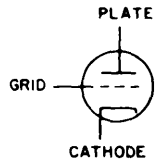
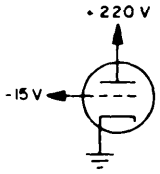
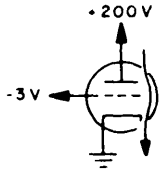
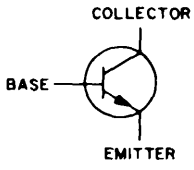
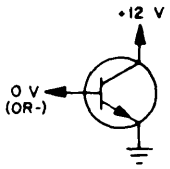
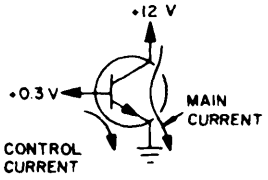
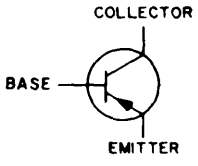
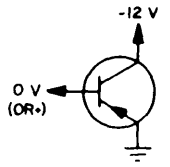
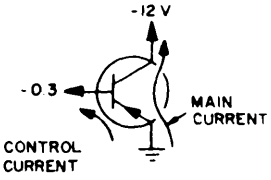


Figure 9. Typical Diode Gate Circuit Functions.

A. TRANSISTOR BIASING

DEVICE	SYMBOL	CUTOFF	CONDUCTING
VACUUM TUBE			
NPN TRANSISTOR			
PNP TRANSISTOR			

B. AMPLIFIER CHARACTERISTICS

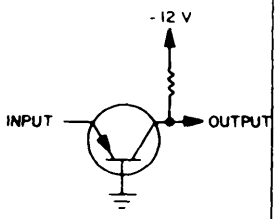
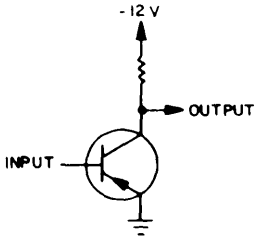
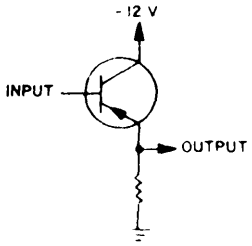
CHARACTERISTIC	COMMON BASE	COMMON EMITTER	COMMON COLLECTOR
INPUT Z	30-50 Ω	500-1500 Ω	20-500K Ω
OUTPUT Z	300-500k Ω	30-50K Ω	50-1000 Ω
VOLTAGE GAIN	500-1500	300-1000	<1
CURRENT GAIN	<1	25-50	25-50
POWER GAIN	20-30db	25-40db	10-20db
			

Figure 10. Transistor Operation.

(1) In the flip-flop shown ill Figure 11A, Q2 is initially conducting. A near-zero voltage is supplied to the base of Q1 front the R7 and R1 voltage divider. The ratio of the divider is such as to make the base voltage only slightly negative, to hold Q1 cut off. With Q1 cut off, the R6-R3-R2 divider delivers a negative voltage to the base of Q2 to keep it conducting.

(2) The flip-flop is initially set by a negative reset pulse applied to the base of transistor Q2. Diodes CR1 and through CR4 serve as steering and clamping diodes. The input pulses are then applied to the bases of transistor Q1 and Q2 through capacitors C1 and C2 and steering diodes CR1 and CR3 which act as inhibit gates to the transistors. The reset pulse sets Q2 to conduct enabling the gate for Q2. The trigger pulses are differentiated by capacitors C1 and C2 to develop a negative and a positive pulse. The pulses are applied through the steering diode that is enabled to the related transistor base.

(3) At time t_2 the positive input pulse cuts off Q2; the Q2 collector voltage goes negative and drives Q1 into conduction (R1-R7 divider to Q1 base); the Q1 collector voltage and the Q2 base voltage (R2-R3 divider) then become considerably less negative, holding Q2 cut off. In a similar manner the positive input pulse at time t_4 cuts off Q1 and a similar sequence of events takes place which ends with Q2 conducting and Q1 cut off. Note that a negative input pulse has no effect due to the steering diodes.

l. Binary Circuit. In this manual a flip-flop which completes its operating cycle and produces an output pulse after receipt of two similar input pulses is called a binary circuit. The binary circuit is driven from a single input which is connected either through a pair of resistors or through a pair of gating diodes to each transistor base.

m. Trigger Circuit. The trigger circuit is a squaring amplifier which produces an output waveform with very fast rise and fall times. Initially in the circuit shown in figure 1113 the input voltage is positive and (1 is therefore cut off. The negative voltage applied to the base of Q2 through the R2-IR: f-R4 divider causes Q2 to conduct heavily. The output voltage (Q2 collector) is therefore only slightly negative.

(1) At time t_1 the input signal becomes sufficiently negative to drive Q1 into conduction. The voltage at the Q1 collector and the Q2 base (through the R3-R4 divider) becomes less negative and reduces the conduction of Q2, reducing the voltage drop across R5. The Q1 emitter-base forward bias increases to cause still heavier Q1 conduction. Action stops when Q1 is saturated and Q2 is cut off. Capacitor, C1 bypasses R3 to couple fast changes in voltage at the Q1 collector to Q2 base.

(2) At time t_2 the input voltage goes positive and Q1 conduction is reduced. Both the Q1 collector voltage and the Q2 base voltage go negative and Q2 comes into conduction. Current flow increases in the R5, Q2, and R1 voltage divider chain. Q1 goes into cut off as the emitter-base forward bias is reduced.

n. One-Shot Multivibrator. The one-shot or monostable multivibrator is a circuit which generates a pulse of some specified duration following the application of a suitable triggering pulse.

(1) In the typical one-shot multivibrator shown in Figure 11C the following conditions exist during the initial stable period. The R1-R5 divider delivers a sufficiently negative potential to the base of Q1 to hold Q1 in saturation. The Q1 collector is therefore only slightly negative. The R2-R3-R4 divider delivers to the Q2 base a slightly positive voltage to hold Q2 cut off.

(2) The positive triggering pulse at time t reduces conduction of Q1. The resulting negative-going voltage at the Q1 collector is applied to the base through the R2-R4 divider (C2 bypasses R4 to provide coupling for the rapidly changing voltage at the Q1 collector). Q2 begins to conduct. The resulting positive going change in Q2 collector voltage is coupled through C3 to the Q1 base and further decreases Q1 conduction. The process is regenerative and quickly results in Q1 being cut off and Q2 being saturated.

(3) Capacitor C3 no, charges at a rate mainly determined by the values of R5, R1 and C3. When the Q1 base voltage becomes sufficiently negative, Q1 begins conduction. The resulting positive-going Q1 collector voltage is coupled to the Q2 base. The Q2 collector voltage goes negative and is coupled through C3 to the Q1 base and further increases Q1 conduction. The process is regenerative, and en(is with the circuit in its original quiescent state (Q1 saturated and Q2 cut off).

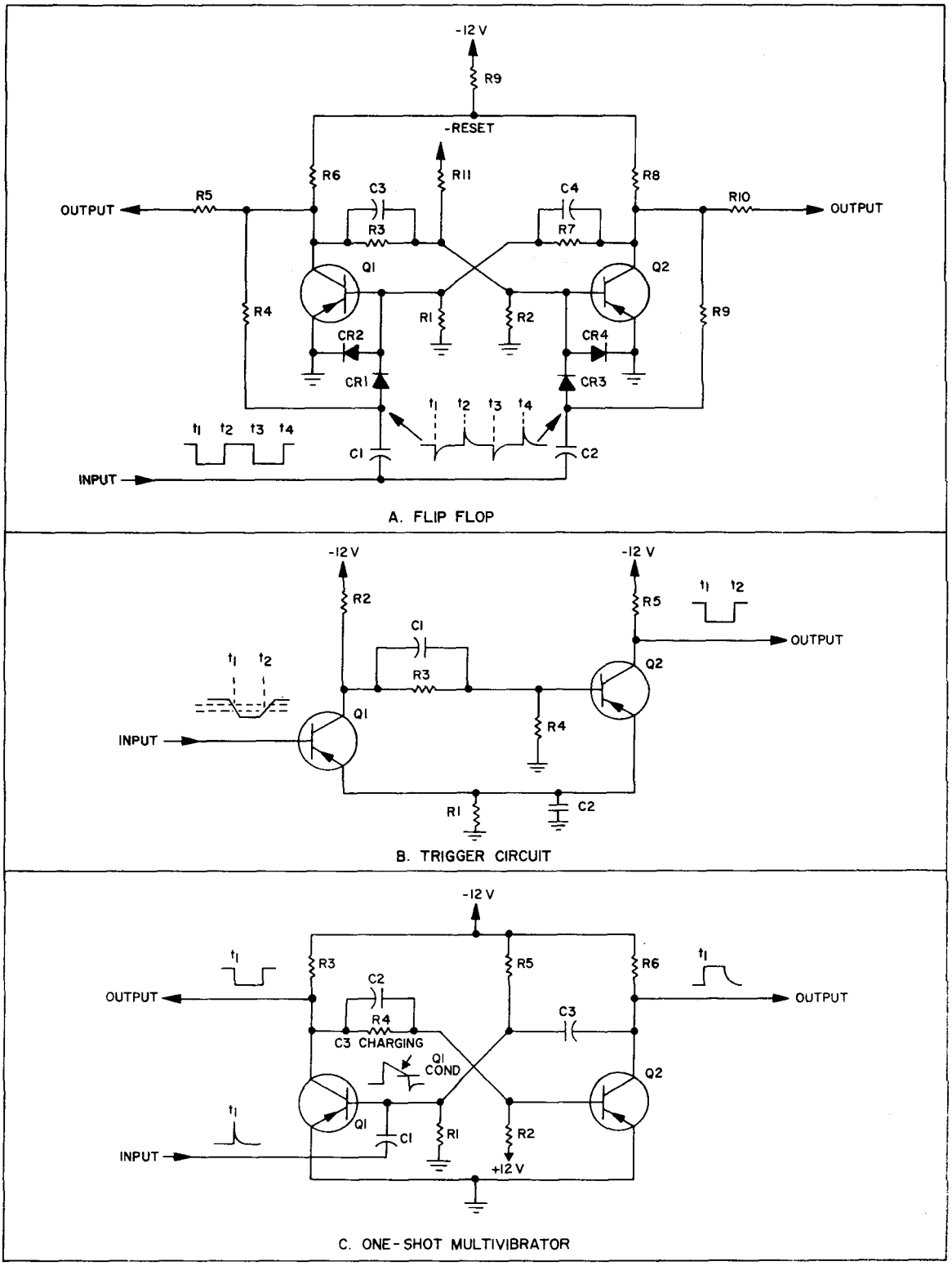


Figure 11. Basic Transistor Circuits.

o. Decade Counter Basic operation. Operation of the decade counter circuit and the decade divider circuit is similar. The difference between the two circuits is in their function. The decade counter circuits accumulate the count to be applied to the digital display tubes. The divider circuits are used to divide the output from the internal oscillator into the frequencies to be counted or into the frequencies that provide the various gate times. Throughout the following discussion circuits are referred to as counters although the description applies equally to decade dividers. Paragraphs 22 o (1) through 22 o. (5) cover general operation of the counters with emphasis on counting logic, and Paragraphs 22 o (6) and 22 o (7) discuss readout circuits.

(1) Input and Output from Binary. Figures 12A and 12B show a flip-flop connected for operation as a binary circuit (basic flip-flop operation) is discussed in Paragraph 22k. Positive input pulses are applied to the bases of both transistors and causes switching by cutting off the conducting transistor. Negative reset pulses go to the base of one transistor and turn it on. Note the letter A near one transistor and X (read as A bar or not A) near the other transistor. The positive-going transition at the collector of the A transistor (while switching from t conducting to A conducting) provides the input to the next binary circuit.

(2) Circuit Arrangement and Count Notation. Figure 12C is a block diagram of a typical four-binary decimal counter, Notice that the A output is applied to the B, ;, and D transistors and that the C output is applied only to the 1 transistor. Each input pulse produces a different combination of conducting and cut-off stages. There are only 10 allowable combinations and each combination represents a decimal digit. Decimal weighting is the decimal value assigned to the output of a pair when the plain-letter transistor is conducting.

(a) Decimal Count. Decimal weighting used in the display indicator is shown in Figure 12C immediately above each of the four binary stages. The decimal weight each pair represents is present only when the barred-letter side (A, B, C, or D is conducting. When the plain-letter side (A, B, C, or D) is conducting, the decimal weight is zero. The decimal count can be determined by adding the decimal weighting of the four stages.

(b) Binary-Coded Decimals. In binary-coded decimal notation, the output is either 1 (when the barred letter transistor is conducting) or 0 (when the plain-letter transistor is conducting). In binary coded decimal notation, the order of the binaries is given so that binary-cod(,d decimals can be written with the least significant digit to the right. Thus, in the system used in the display indicator the binary coded decimal notation normally is given in the order DCBA. (Counter binaries are shown in the ABCD order on the schematic(s and in Figure 12C to increase clarity in showing signal flow.)

(3) Sequence. Figure 13 shows the counting sequence for a typical decimal counter. Refer to 25-MHz decade counting unit schematic for circuit location of components referred to. The 2.5MHz and 250-KHz decade counting units circuits are similar except the do not contain the second gate circuit before the fourth binary. Initially after, 'each binary is in the () state (decimal count = 0, DCBA (000). The following action takes place when a: series of input pulses is applied to the counter.

(a) The first pulse switches A binary to the 1 state (DCBA = 0001).

(b) The second pulse switches A binary to the 0 state. The output from A binary is applied through emitter follower A11Q10 to the AND gate input of B binary. Diode A11CR32 applies an enabling voltage to the AND gate. This permits diode A11CR8 to pass the output from A binary to switch the B binary to the 1 state (DCBA = 0010). The output of the B binary is AND gated with the A and C binaries (A11CR15, A11CR16, A11CR23) to provide an input gate to the D binary.

(c) The third pulse switches A binary to the 1 state (DC13A = 0011).

(d) The fourth pulse switches A binary to the 0 state. The output from A binary switches B binary to the 0 state. The output from B binary switches the C binary to the 1 state (DCBA = 0100).

(e) The fifth pulse switches A binary to the 1 state (DCBA = 0101).

(f) The sixth pulse switches A binary to the 0 state. The output from A binary switches B binary to the 1 state (DCBA = 0110).

(g) The seventh pulse switches A binary to the 1 state (DCBA = 0111).

(h) The eight pulse switches A binary to the 0 state. The output from A binary switches B binary to the 0 state. The output from the B binary switches the C binary to the 0 state. The switching of the three binaries switches D binary to the 1 state (DCBA = 1000). Since the B binary input AND gate is enabled by the D binary, the switching of the D binary now inhibits the 13 binary gate, but also, enables the nine-carry gate function (A11CR30 and A11CR31).

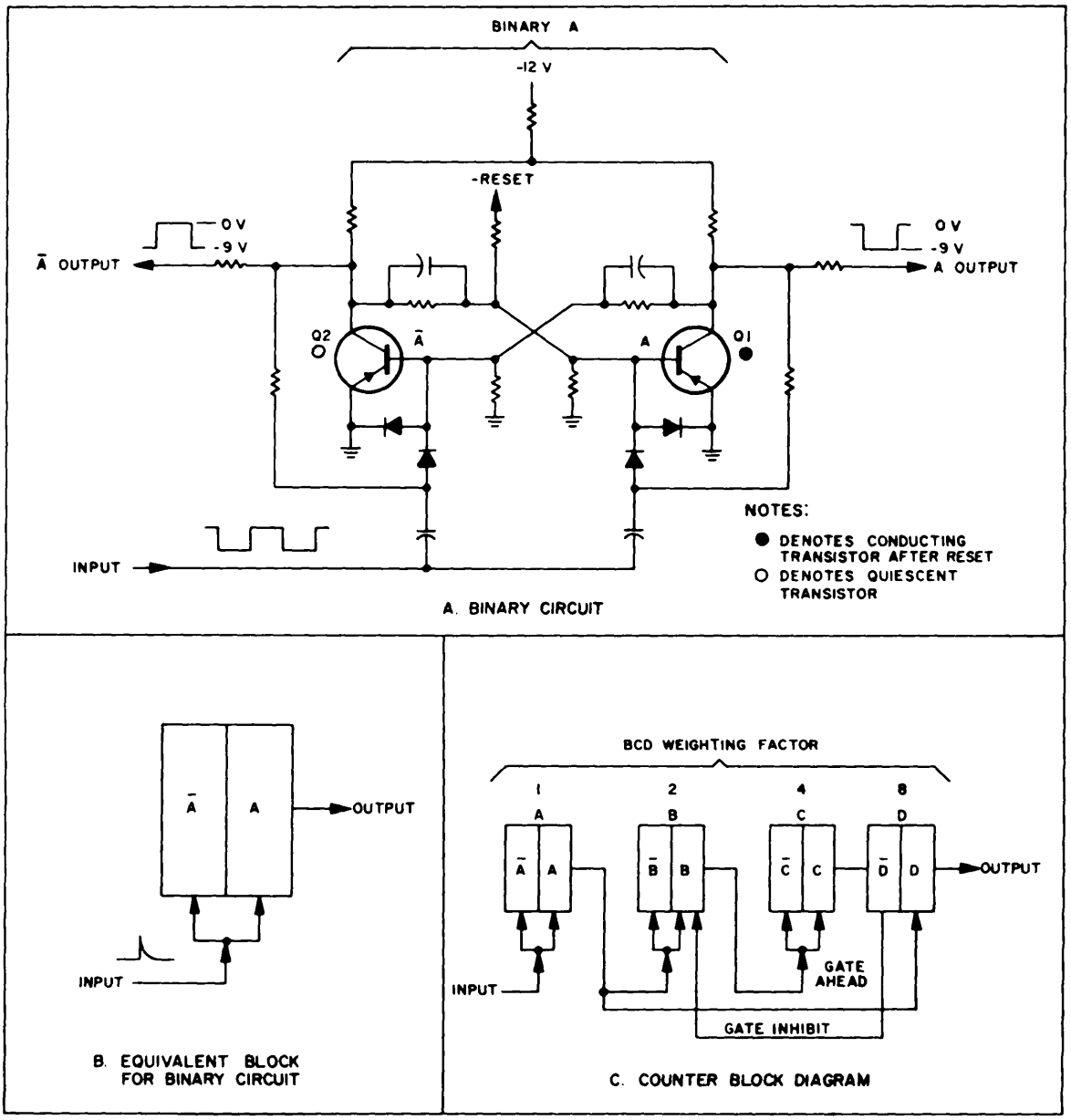


Figure 12. Basic Four Binary Counter.

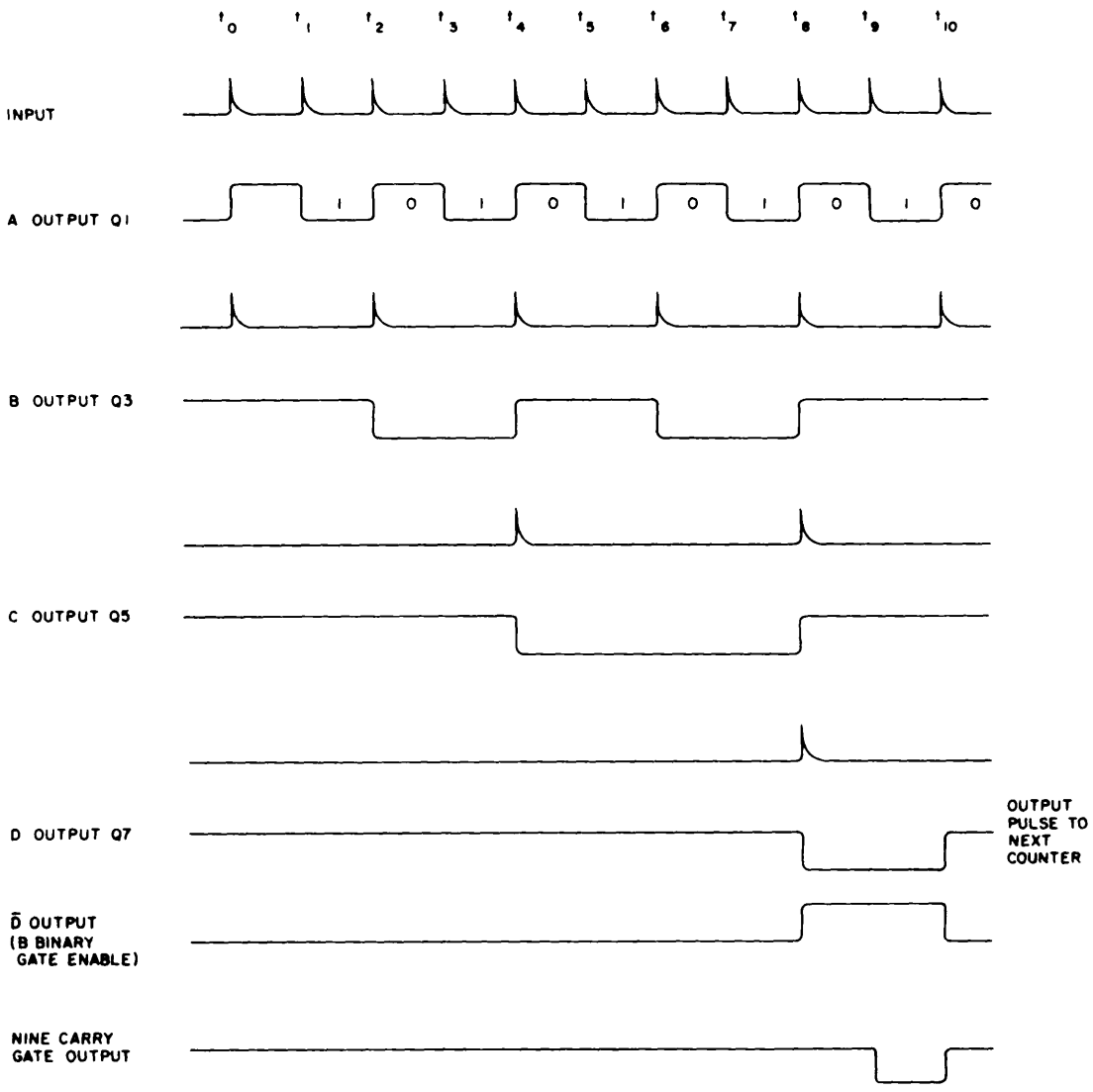


Figure 13. 25-MHz Decade Counting Unit, Timing Functions.

(i) ninth pulse switches A binary to the 1 state. The output from A binary is applied to nine-carry AND gate through diode A11CR31. This provides a pulse to the nine-carry line. Since the nine-carry gate was enabled by D binary, the ninth pulse also causes an output pulse to occur from the nine-carry line (DCBA 1001).

(j) The tenth pulse switches A to the 0 state. The output from A binary is applied as a gateahead pulse to the D binary (through capacitor Al1C18) and switches D binary to 0 state (DCBA = 0000).

(k) The switching of the D binary to 0 causes an output pulse to be generated by the counter circuit which is applied to the next counter signifying ten pulses were counted.

(4) Resetting to Zero. The reset pulse (negative) is applied to the base of the 0 state transistors (A, B, C, and D in each binary circuit. If the 0 state transistor is not conducting, the pulse sets it on. In this manner the reset pulse ensures that all four 0 state transistors are conducting. Decade dividers can be reset as required to any desired state, since reset inputs are available at each transistor. Note the difference between a regular input signal is positive-going and causes a conducting transistor to cut-off; a reset pulse is negative-going and causes a cut-off transistor to conduct.

(5) Timing. Waveforms showing time relationships for the electronic counter are shown in Figure 13. Note that a driven binary switches only when the input wave is going positive.

(6) Electrical Readout. A four-line binary-coded-decimal output is available from the decade counter assembly. A voltage representing the state of each binary is taken from the collector of each of the plain-lettered transistor (A, B, C, and D). A binary 1 is represented by a negative voltage (-9 volts) on each line. A binary 0 is represented by a relatively positive voltage (-0.3 volts) on each line. Table 5 summarizes the ten allowable combinations which represent the decimal digits 0 through 9. (To protect the binary circuit from being effected by the load, each output line contains a 6800 ohm series-connected resistor which is not located on the printed circuit board.)

(7) Digital Display. A display matrix, containing a glow tube and associated decoding network, is used to convert the binary code representation to a decimal numerical representation. Refer to memory readout circuit, Paragraph K for a discussion of decimal display functions.

(8) Presetting Count. A count preset circuit (containing a pulse generator and gating diodes) is used to set an offset count into the counters. The count is equal to the receiver's intermediate frequency offset frequency. The preset pulse functions in a similar manner as the reset pulse, except that it is applied only to the counter binaries that are used in the frequency counter chain.

Section II. PRINCIPALS OF OPERATION

23. General

This section contains the principals of operation of the electronic counter circuits. Included is a simplified block diagram discussion and a detailed block diagram discussion for the circuit functions.

24. Frequency Measurement Technique

a. The electronic counter is a wide-band high frequency counter used to measure the output frequency of the local oscillator of a radio receiver. The electronic counter uses a frequency sampling process for frequency measurements. Use of a sampling technique permits greater frequency measurement range capability. Also, frequency measurement time is reduced as compared to other methods.

b. The sampling technique is a process by which a lower frequency replica of a repetive input waveform is produced by 1) measuring the input waveform amplitude for brief periods at selected points along the waveform and, 2) arranging these points to uniformly advance in phase. In this manner the cycle is ultimately covered with reasonable definition. The steady advance of the sampling points is called stewing. When the sampling technique method is applied to a frequency counter, it is only necessary to make a go-no-go decision as to whether the input signal is above or below the baseline reference point. That is, since the important factor is the counting of the frequency cycles and not in dispalying a faithful replica of the waveform, the number of samples-per-cycle can be fewer than are required in sampling oscilloscopes. (See fig. 14).

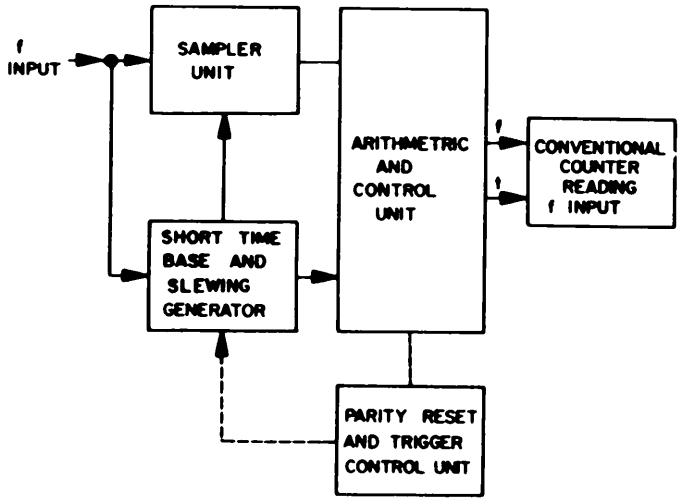


Figure 14. Sampler Counter, Block Diagram.

c. The sampler unit effectively slows down the frequency of the input signal (F input) by several orders of magnitude. In order to determine F input the time base must be slowed down proportionally. If a conventional time base length such as one second were slowed down by the same factor as F input measurement time would be impractically long. Therefore, the short time base and slewing generator produces a very short time base which can be slowed down without introducing an excessive measurement time. The generator simultaneously controls the slewing rate of the sampling process.

d. Mathematically the sampler unit output signal, the length of the short time base and the slewing rate contain all the information required to determine the input frequency. These signals are therefore fed into the arithmetic and control unit which performs a number of arithmetic operations and generates a relatively slow output signal with frequency "f" and time duration "t". The key to this procedure is that "f" is related to "t" in exactly the same way the F input would be related to a conventional time base. Thus, these signals, when presented to the conventional counter, will read out a number which is a direct measure of F input.

e. The last unit, the parity reset and trigger control, does not enter into the frequency counting process, but it does contribute to the accuracy and simplicity of operation. Parity check, a known process in digital computers, has never been used in digital counters before. In effect this circuit monitors the consistency of the readings, and if the consistency criteria are not met (as is the case when the input signal is excessively noisy, too weak, or falls outside the frequency range of the instrument), parity resets the counter and presents an all-zero reading or the preset reading on Bands I, H, m and IV. If the instrument is operated in the auto-trigger mode, the parity check circuit also controls the trigger level until a stable trigger point is obtained.

25. Simplified Block Diagram

The electronic counter circuits are arranged in seven basic circuit functions. The input circuits, the 1-MHz clock circuits, the control and ranging circuits, the time base generator circuits, the parity check circuits, the preset circuits, and the totalizer (or counter) circuits. The energized conditions of three relays in the control and ranging circuits will determine the frequency bands to be used. (See fig. 15.)

a. Input Circuits. The input sampler unit consists of the input coaxial switch and power divider assembly, the I.C . circuit, the S.C. circuit, the F. S. circuit, and the I.S. circuit (see fig. 16). The coaxial switch and the power divider route the display indicator input signals to the input sampler unit circuits.

(1) The receiver output signals supplied to the electronic counter are selected by the energized or deenergized condition of the coaxial switch and applied to the power divider. The power divider routes the input signal to the I. C. circuit and the I. S. circuit.

(2) The input frequency is applied to the I. C. circuit with the N-Ratio level voltage generated by the ramp generator circuit. The I. C. circuit processes the two signals to develop the signal ratio of 4f/N. This 4f/N signal is applied to the S. C. circuit for further processing producing the f/N signal at its outputs.

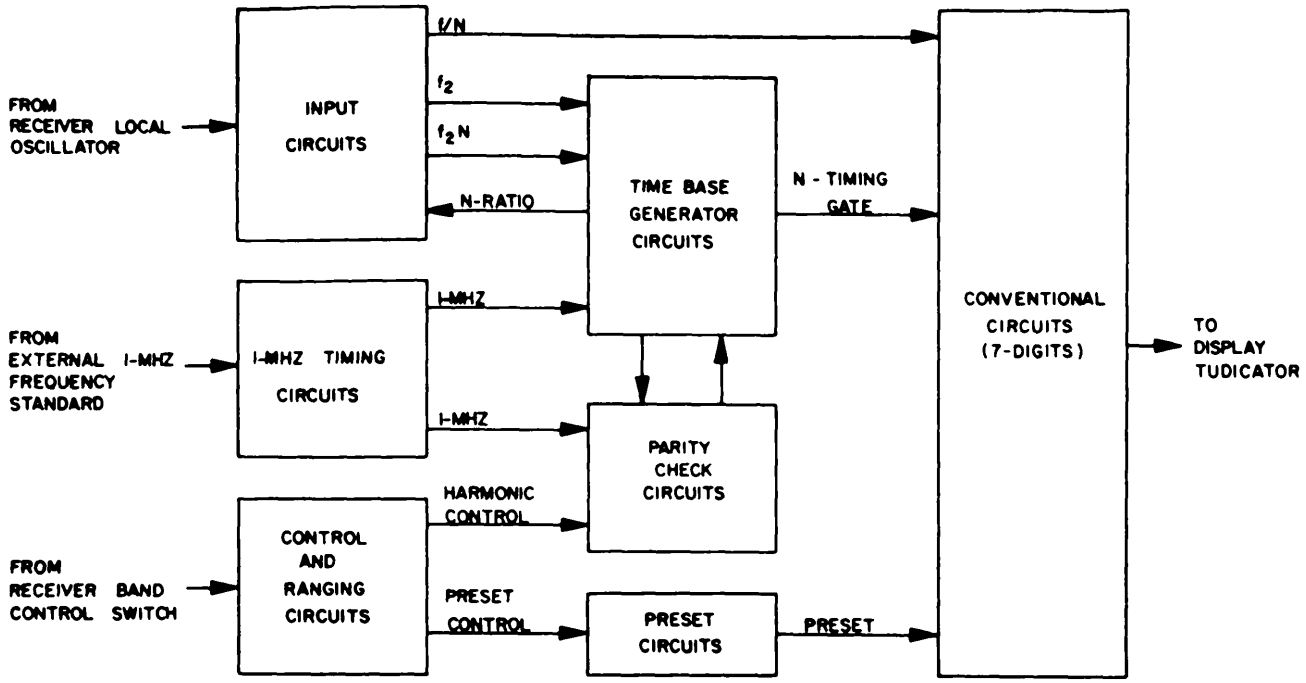


Figure 15. Display Indicator, Simplified Block Diagram

The f/N signal (N-Count) is then applied to the F. S. circuit and the C. U. circuit. Also supplied to the C. U. circuit is the N-Timing gate. Due to the control action of the N-Ratio level voltage applied to the I. C. circuit, the f/N signal will be a continuous signal that is a ratio to the f-input frequency.

(3) The F. S. circuit generates a short time base signal f_2 frequency 1.5 KHz and also after further processing of the f/N signal (supplied from the S. C. circuit) applies the f/N + f_2 signal to the I. S. circuit.

(4) The input f-frequency, supplied from the power divider, is processed in the I. S. circuit with the signal supplied from the F. S. circuit to develop the f_2N signal is a continuous signal which is then applied to the ratio gate circuits with the ratio gate pulses for processing.

b. Counter Circuits. The decimal counting circuit consists of a C. U. circuit, a matrix circuit, six decade counting unit circuits and seven memory readout circuits (see fig. 16). The f/N signal (generated in the S. C. circuit) is applied to the C. U. circuit and is counted for the duration of the N-Timing gate. (The N-Timing gate is supplied from the time base generator ratio and control circuits.) The states of the C. U. circuit and the decade counting unit circuits are applied to the memory readout circuits for final decimal display.

(1) The C. U. circuit is a high-speed counter circuit which divides the input N-Count by ten and supplies an output to the six decade counter units for accumulating. The C. U. circuit final-count states are applied to a memory readout circuit through a matrix circuit decoder.

(2) The matrix circuit amplifies the C. U. circuit final count states and also converts the quinary input count to a binary coded-decimal code (BCD) through a decoder circuit. The BCD code is then applied to a memory readout circuit for display.

(3) The C. U. output is accumulated by the decade counter units which serve as binary-coded-decimal dividers. The input pulses are divided down by ten in each counter during the enabling interval of the N-Timing gate. The closing of the N-Timing gate by the stop flip-flop stops the accumulating function. At this time a display and read pulse are generated.

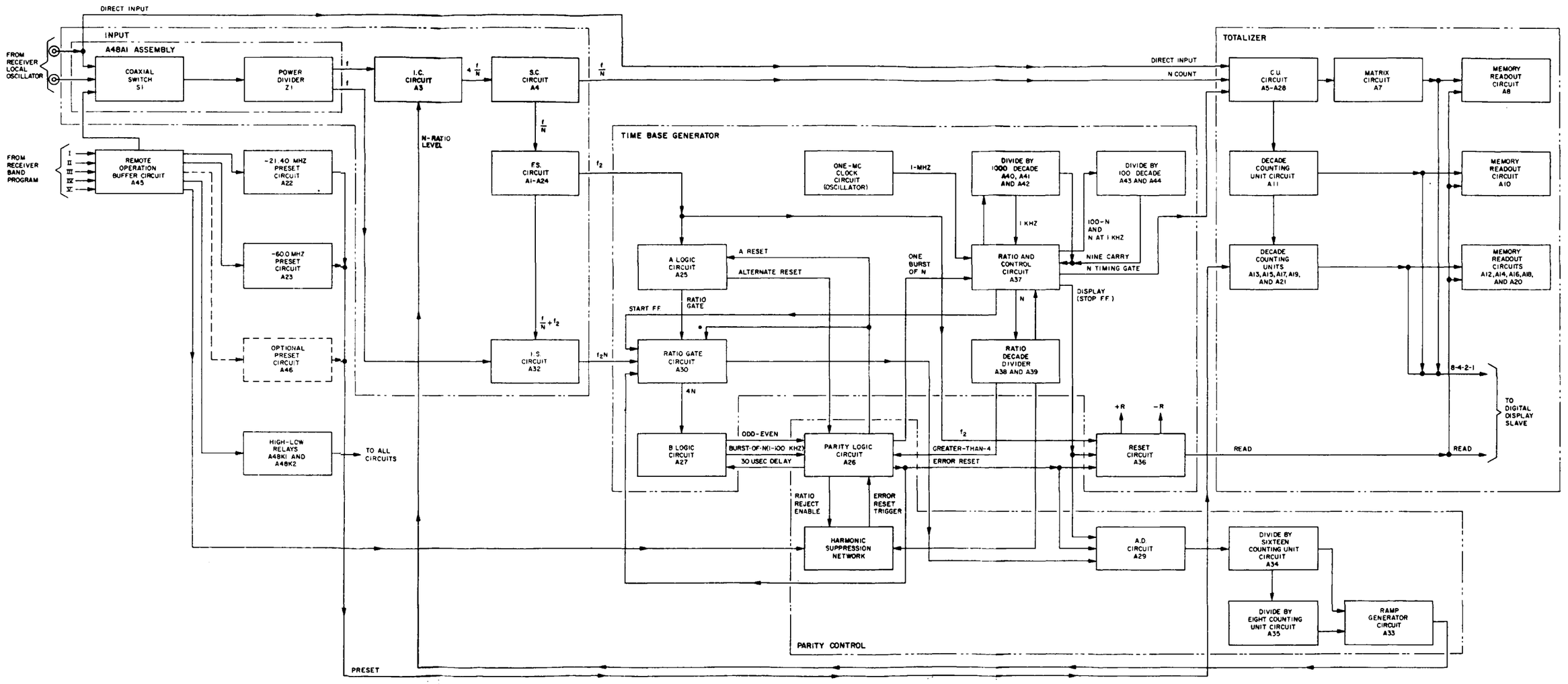


Figure 16. Electronic Counter, Detailed Block Diagram

(4) The read pulse generated by the reset circuit display timer is applied to the memory readout circuit. The read pulse transfers the decade counter unit final-count states to the memory readout circuit. The memory readout circuit causes a display of the accumulated N-Count on the glow-tube readouts. These displays are representative of the decimal N-Count in the associated decade counter unit circuits. Each totalized N-Count set into the readout display is held until the next read pulse changes the input flip-flop states of the memory readout circuit.

(5) If the parity circuits determine that a consistency error exists, (due to noise, inadequate or changing input signals or a malfunction), the parity circuits will cause the memory readout circuit to display the preset frequency. This frequency will be equal to 10,000.000 MHz less the receivers intermediate frequency (that is, 10,000.000 MHz Iess 60.0 MHz equals 9940.000 MHz). This resultant frequency is the IF offset. If the receiver output is normal (within the operating range of the channel selected) and the programmer control is functioning properly, continuous display of the IF offset is indicative of a malfunctioning electronic counter. The IF offset will be displayed until the parity circuit determines that a consistent frequency measurement is accomplished and no error pulses are generated.

c. Parity Consistency Check. The parity logic circuit monitors the frequency measurement, performing consistancy checks of the electronic counter computation circuits. Several successive frequency measurements are compared, the number being determined by the setting of the rear panel PARITY control. To prevent performing false measurements or displaying incorrect measurements, harmonic suppression network is use(to limit the lower and upper frequencies to be measured by a band selected. (This control does not function on band V since most of this band will contain harmonic frequencies.)

(1) The purpose of the parity check is to inhibit the false measurements. Therefore the error reset will occur only during false measurements. No output signal will occur during accurate measurement checks. If the frequency measurement consistency check comparisons are dissimilar (caused for example by noise or the local oscillator output frequency changing as the radio receiver is being tuned) the results of the confidence check will signify a consistency error and an error reset pulse will be generated. The error reset pulse generated is applied to the reset circuit, the A. D. circuit, and the memory readout circuit. This will cause the display to show the IF offset preset number as described previously in paragraph 25b (5).

(2) The A. D. circuit develops a trigger pulse that is applied to the ramp generator circuits. If three error reset pulses are successively generated, the A. D. circuit generates a pulse to cause the ramp generator circuit to step to a new N-Ratio level. The N-Ratio level, applied to the I. C. circuit, causes the I. C. circuit to change to a new ratio.

(3) The harmonic suppression network serves to sense the frequency harmonic ratio at a certain level and causes the parity logic circuit to reject any measurement above the preselected level. The electronic counter is designed to measure reasonably pure sinusoidal continuous wave signals. Although a distorted signal rich in harmonics may be measured, it will cause frequent consistency error indications and may display the harmonic frequency instead of the fundamental frequency. The harmonic suppression circuit is designed to provide control functions that minimize tracking in the harmonic signal range for a specific band selected. This is accomplished by the rejection of any measurement above the preselected maximum frequency for the range. This causes a pulse to be generated which is sent back to the parity logic circuit to trigger the one-shot circuit. Occasionally if a harmonic of a signal falls within the frequency range selected, the harmonic suppression network cannot detect it, and it will be displayed. The result will be a momentary change of the frequency displayed and then the correct frequency will be displayed again.

d. Time Base Generator Circuit. The time base generator circuit is referenced to the 1-MHz crystal oscillator (see fig. 15 and 16) and serves as the timing reference for all timing functions (see fig. 17). The oscillator 1-NMliz output frequency is divided down through three decade counters to develop a precision 1-KHz pulse output. The 1-KHz pulse output is applied to two additional decade counters to develop a 10 hertz pulse. The nine-carry function from the five decade counters are AND'ed together and applied as a trigger pulse to the start-stop flip-flop circuits (N-Timing gate) of the ratio and control circuit. The N-Timing gate pulse width, developed by the time base generator circuit, is controlled by the ratio decade dividers. Since the N-Timing gate pulse width is a function of the N-Ratio determined by the I. C. circuit and the frequency being measured, the pulse width will vary for different frequencies.

e. Control and Ranging. The energized or deenergized states of relays A48K1 and A48K2 determines the operating ranges for the various circuit functions. The remote operation buffer circuit is supplied program control signals from the receiver used with the electronic counter to automatically energize the relays or the coaxial switch. In addition, the remote operation buffer circuit provides the enabling functions that selects the intermediate frequency offset required for the receiver band used.

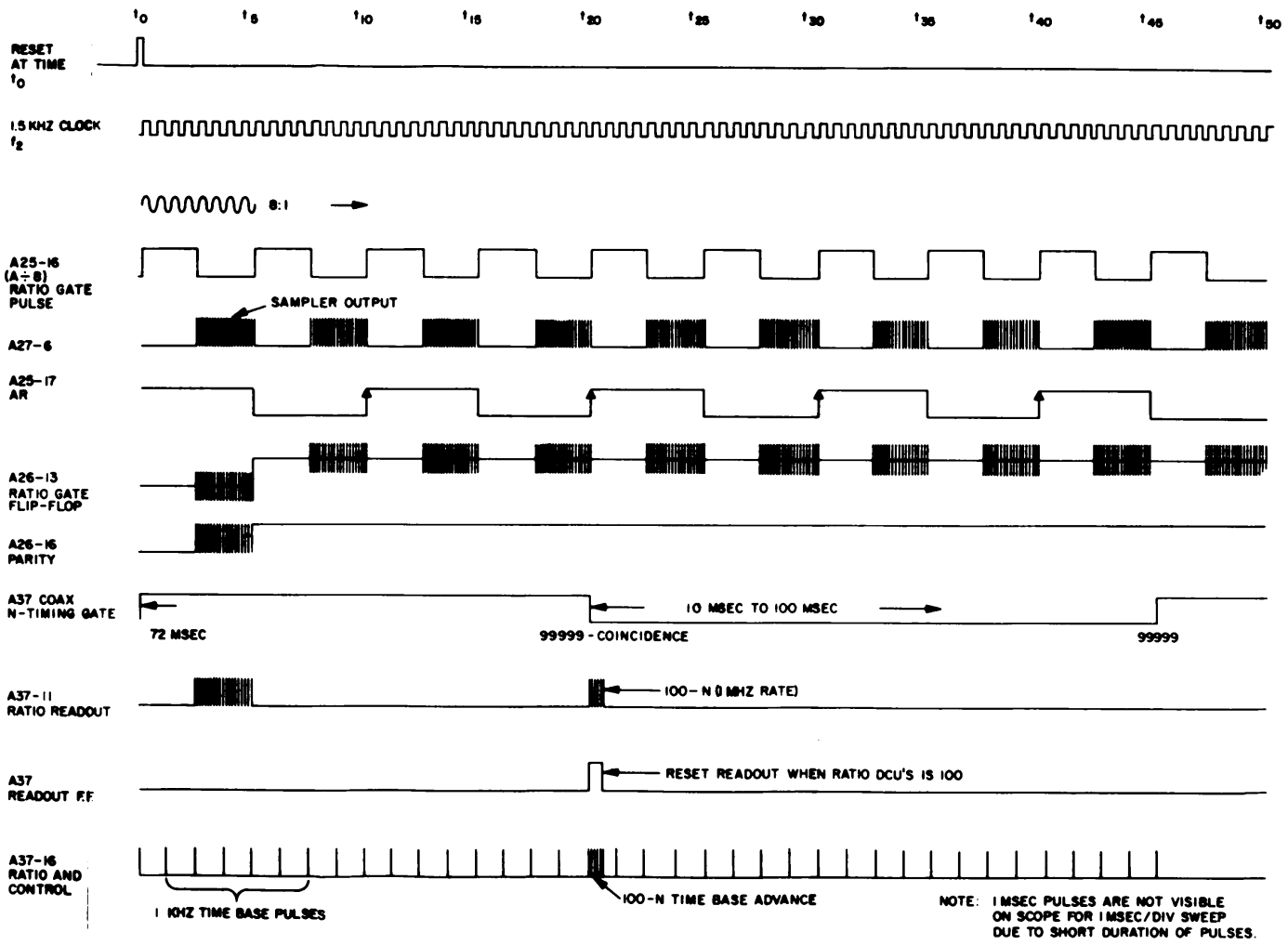


Figure 17. Time Base Generator, Timing Functions

f. Preset Selection. Prior to accumulating an N-Count, a preset generator circuit is enabled by the preset pulse to enter the IF offset into the decade counting unit circuits. The preset IF offset is now subtracted from the incoming N-Count. The resultant frequency will be the correct N-Count computation and is fed to the memory readout circuits for display.

26. Detailed Block Diagram

a. The basic counter circuit functions are arranged to provide two modes of operation. Each arrangement includes a main gate with 1) a signal input and 2) a control input or gating signal. Following the main gate is a cascade series of decade counters which accumulate and display the total number of pulses that are passed during the enabling of the gate. (See fig. 16.) The modes of operation are discussed in paragraph 27.

b. Circuit operation in the two modes is similar. Pulses are passed through the main gate to the decade counters for a predetermined period. The pulses are counted and the measured frequency is displayed by the readout indicator. The primary difference is the method used to maintain a consistent accuracy check of the input frequency. (At frequencies below one hundred mega-hertz, the parity check circuit is bypassed.) The two operating modes are relay selected by external programming generated in the receiver used with the electronic counter. The readout decimal point position is fixed and the measured frequency display is read in megacycles.

27. Operating Modes

a. Direct Mode. In the direct mode of operation, the electronic counter functions as a conventional frequency counter. The decimal counters count the total of input pulses while the timing gate is held open. The count in the decade counters is then transferred to the readout circuit for display. During normal operation, the local oscillator output frequency from a receiver is applied to the input jacks J1 and J2 (depending on the frequency to be measured as listed in Chapter 1) of the electronic counter input circuits. If the signal is applied to J1 (1KHz to 100 MHz), the remote operation buffer circuit is simultaneously programmed to actuate relay A48K1. The relay is used to disable the electronic counter input and parity control circuits during low frequency measurements. The signal applied to J1 is then routed directly to the C. U. circuit as a direct input where it is totalized. This operation is called the direct mode.

b. High-Low Modes. In either the high or low mode of operation (see fig. 16) the electronic counter circuit arrangement permits control of the N-Timing gate by the cascade counter time base generator circuit. (The high and low modes function in a similar manner except for the frequency coverage.) The N-Timing gate is opened for a controlled time interval (N-Timing period) and the accumulated count in the decimal counters re- presents the number of input cycles or pulses passed. The controlled intervals (width of the N-Timing gate) will vary for the frequency being measured (from something more than 1 millisecond to something less than 100 milliseconds). The intervals are automatically determined by the time base generator circuit.

28. Direct Mode Frequency Measurement Cycle. (See fig. 18)

The direct mode frequency measurement cycle is initiated as the reset pulse clears (or sets) all circuits to specific states. The end of the reset pulse sets the preset pulse. A preset generator circuit (-21.40 MHz) is enabled to set a predetermined offset-count into the totalizer counting decades. A set of preset diodes loads the two decade counters to a state other than zero.

a. N-Timing Gate Generation. The direct mode of operation N-Timing gate is generated by the five decade dividers counting down the 1-MHz oscillator output. The oscillator output is squared in a shaper circuit to develop trigger pulses for the divide-by-ten dividers. The pulses are divided by the first three decade dividers and then routed through an OR gate to two additional dividers. At a nine-carry coincidence output of the dividers, the resultant carry pulse generated is applied to the start-stop flip-flop circuit input.

b. Start-Stop Flip-Flop Output. The negative-reset pulse resets the states of the start and stop flip-flop circuits to a predetermined condition. The action enables the circuits to react to the nine-carry pulses generated by the decade dividers. (The nine-carry pulses are constantly being generated but will not trigger the start-stop flip-flops until their gates are enabled. Simultaneously with the resetting of the start-stop flip-flops, the first three dividers are reset to zero while the positive-reset the last two dividers to a predetermined count. This count serves to speed-up (or advance) the carry coincidence of the dividers outputs to the start flip-flop. Since the five dividers will be coincident every 100 milliseconds, the advancing of the coincident condition decreases the time interval after application of the reset pulse to 72 milliseconds before the first carry pulse. The first carry pulse to occur after reset, sets the start flip-flop, resulting in the opening of the N-Timing gate. Due to the 1-MHz frequency and the amount of dividers, the resultant time interval between the first carry pulse and the arrival of a second carry pulse will be 100 milliseconds long. The setting of the start flip-flop also enables the stop flip-flop gate and inhibits the start flip-flop gate. The arrival of the second carry pulse (100 milliseconds later) sets the stop flip-flop. The resultant action closes the N-Timing gate.

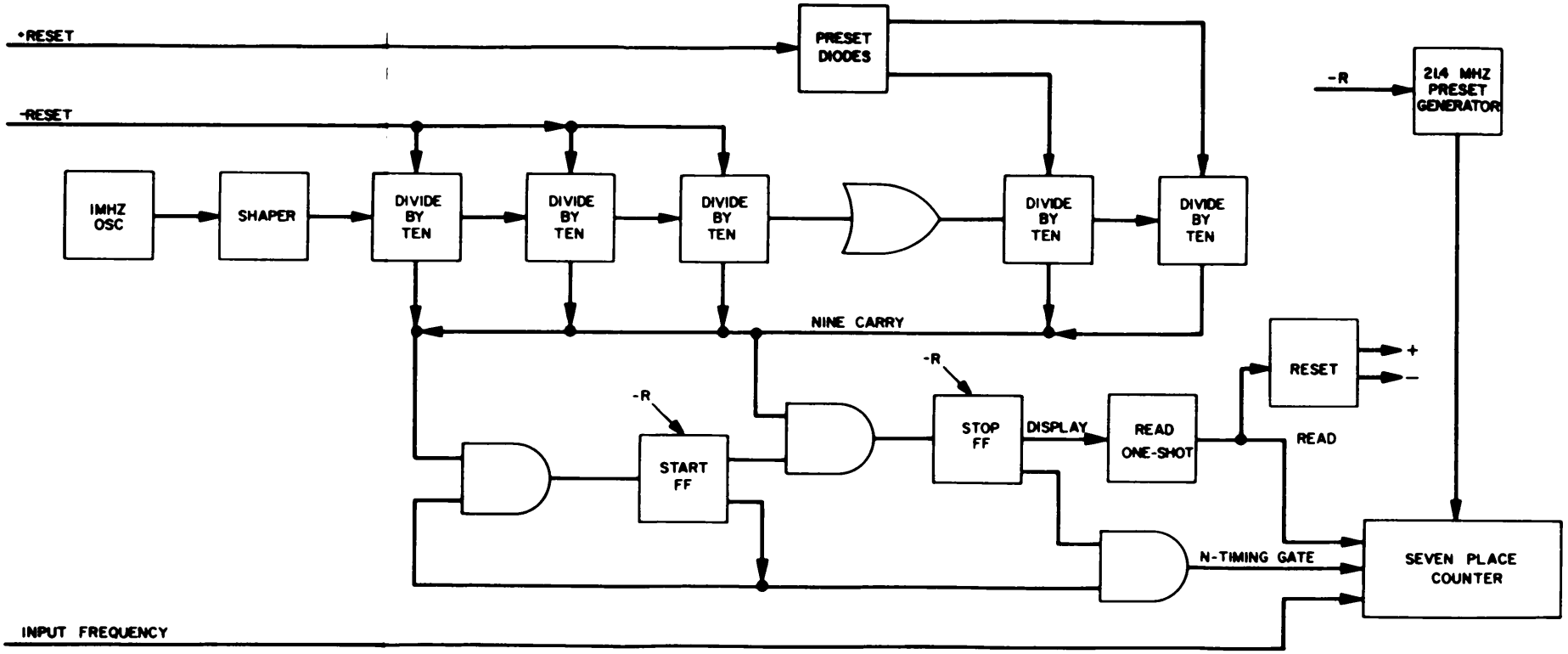


Figure 18. Electronic Counter, Direct - Mode of Operation, Block Diagram

c. C. U. Circuit Gating. The N-Timing gate generated by the start-stop flip-flops is applied to the C.U. circuit as a gating pulse. The input frequency at J1, which is also applied to the C.U. circuit input, is counted by the counting chain during the interval the N-Timing gate enables the C.U. circuit input.

d. Totalized Count Display. The totalized count in the counter circuit is transferred to the memory readout circuits as a result of the display pulse generated by the stop flip-flop. The display pulse sets the read one-shot multivibrator which generates the read pulse. The read pulse then provides the transfer function to the memory readout circuit.

e. Reset. After a measurement cycle, it is necessary to generate a reset cycle. Setting the stop flip-flop initiates the reset cycle.

29. High-Low Mode Frequency Measurement Cycle. (See fig. 16.)

a. Input. The external frequency is initially processed by the electronic counter input circuits as described in Paragraphs 25 a and b. The high and low mode frequency measurement operations is similar except certain circuits are disabled or enabled to extend the operating frequency coverage range of the instrument.

b. Ratio Gate. The continuous f_2N signal (supplied by the I. S. circuit) is applied to the ratio gate circuit (A30-16) for processing by the ratio gate pulse. The f_2 signal generated in the F. S. circuit and applied to the A logic circuit (A25,-(16) is divided by four (in either the high or low modes) and the resultant output pulse is applied to the ratio gate circuit (A30-1:3). The f_2 signal is chopped by the ratio gate pulse to develop 4N pulses which are applied to the ratio gate circuit (A30-13). The $f._2$, signal is chopped by the ratio gate pulse to develop 4N pulses which are applied to the B logic circuit (A27-6). Each bursts of 4N pulse applied to the B logic circuit is divided by four (in either the high or low modes) and the resultant bursts of Ns are applied to the parity logic circuit (A26-17) for processing.

c. Parity Consistency. These single-bursts-of-N are processed in the parity circuit to produce a one-burst-of N output (A26-16). This is accomplished by the gating of the ratio gate flip-flop in the parity logic circuit. Since the ratio gate pulse al)plied to the ratio gate circuit (A30) is a function of the 1.5 KHz f_2 signal, an additional flip-flop (alternate reset) in the A logic circuit divides the f_2 signal once more. The resultant alternate reset pulse generated is applied to the ratio gate flip-flop in the parity logic circuit (A26-14). The alternate reset is exactly twice the time duration of the ratio gate. During the first half of the alternate reset one burst-of-N is gated through to the ratio and control circuit (A37-13) for the development of the time base interval (N-Timing gate). The (-) negative swing of the alternate reset pulse clamps the gate closed, not to open again until a new counting cycle starts, beginning with (-R) reset. The second half of the alternate reset occurs as a second burst-of-N is gated through the "B" logic. This burst does not go to the ratio and control circuit, but combines with the first burst-of-N to determine whether they are odd or even. (If N is always odd or is always even, the result of the addition of the two will always be even.) This addition takes place in the odd-even flip-flop in the "B" logic circuit. Only if one signal is odd (7-21 etc.) and the other is even (8-22 etc.) will there be an odd condition existing in the odd-even flip-flop. The odd condition will then be presented to a two input AND gate, the other input coming from the parity enable circuit. Parity enable occurs for 30 microseconds and at the same time of the (+) positive swing of the alternate reset. If the two pulses are conincident, (the odd-even flip-flop set in an odd condition), an output pulse will be generated by the error reset one-shot and then applied to the reset circuit (A36-8) to interrupt the measurement cycle. If no consistancy errors exist there will be no error reset.

d. Measurement Ratio. The two decade division is used to develop the ratio of the burst-of-N and the time base generator gate generated, and also resets the readout flip-flop in the ratio and control circuit (A37-10). The 1-MHz pulses being divided by decade dividers A40 through A44 would normally automatically initiate the start-stop flip-flop circuits at a predetermined time after reset (see Paragraph 28 b). To assure that a time base width (N-Timing gate) will be long enough and also the ratio to the frequency being measured is correct, the readout flip-flop is set at the start of the N-Timing gate (enabled by the start flip-flop) to enable a gate that permits a certain amount of 1-MHz pulses to be applied to the time base dividers A43 and A44. The amount of pulse passed is determined by the one-burst-of-N signal that is divided by the ratio decade dividers. The same amount of l-MHz pulses are applied to the ratio decade dividers as to the time base dividers, both being determined by the number of N pulses. The resultant action is to advance or speed-up the ultimate count in the ratio and the N-Timing gate decade dividers.

e. Counting and Display. The resultant generation of the N-Timing gate pulse is then applied to the C.U. circuit as described in Paragraph 28 c. The readout display is accomplished as described in Paragraph 28 d.

Section III. UNIT THEORY OF OPERATION

30. General

This section provides the theory of operation of the individual printed circuit boards (except the input circuits), the dc power supply assembly and the associated controlling circuits. The input circuits (see fig. 16) printed circuit boards Al, A3, A4, A5, A30, and A32 circuits design are PROPRIETARY and will not be discussed except for types of output signals obtained where applicable.

31. Circuit Description

The electronic counter circuit functions are discussed in the following paragraphs. Signal paths and wave-forms are shown in the block diagram or on related timing diagrams. For complete circuit details, refer to the printed circuit board schematic diagrams in Chapter 7.

a. I.C. Circuit, (A3). The I.C. circuit processes the f input frequency with the N-Ratio level voltage supplied from the ramp generator circuits to develop the 4f/N frequency that is applied to the S.C. circuit.

b. S.C. Circuit, (A4). The S.C. circuit further processes the 4f/N signal supplied by the I.C. circuit and develops the f/N (N-Count) signal that is applied to the C. U. circuit and the counting circuits. The f/N signal is also applied to the F.S. circuit.

c. F.S. Circuit, (A1). The F.S. circuit generates the f_2 slow time base 1.5 KHz signal used by the reset and A logic circuits. The f/N signal supplied from the S.C. circuit is further processed and applied as the f/N + f_2 signal to the I.S. circuit for further processing.

d. I.S. Circuit, (A32). The I.S. circuit develops the f_2N signal from the f/N + f2 signal supplied by the F.S. circuit and the f input frequency supplied from the power divider assembly.

e. Ratio Gate Circuits, (A30). The ratio gate circuits processes the f2N signal supplied from the I.S. circuit with the ratio gate pulse supplied from the A logic circuit to develop continuous bursts of 4N signal. The 4N signal is applied to the B logic circuit for further processing.

f. C.U. Circuit, (A5). The C.U. circuit processes the f/N signal (supplied from the S.C. circuit) while the N-Timing gate (supplied from the ratio and control circuit) is enabled. The C.U. circuit divides the N-Count by ten and drives the remaining decade counting circuits. The C.U. output is also used by the matrix circuit (A7) and becomes the least significant digit in the display.

g. 25-MHz Decade Counting Unit Circuit, (A11). The 25-MHz decade counting unit circuit is a high-speed binary-coded decimal counter that counts (and divides-by-ten) the one-tenth N-Count output from the C. U. circuit. A block diagram of the 25-MHz decade counting unit is shown in Figure 19. (Refer to fig. 12 for circuit timing.) The decade divider is an arrangement of four cascaded binaries (flip-flops) that generates an output pulse for every ten input pulses. Consequently, when a frequency is applied to the counter input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The output from the first binary is applied to the second binary through an emitter follower and an AND gate. The AND gate is enabled by the state of the fourth binary. The first binary output is again divided by two in the second binary (making a total division by four) and so on with an expected total division of sixteen at the output of the fourth binary. The output from the first, second, and third binary is applied through an AND gate to the fourth binary. This is done so the fast speed of the first binary will switch the fourth binary at a much faster rate.

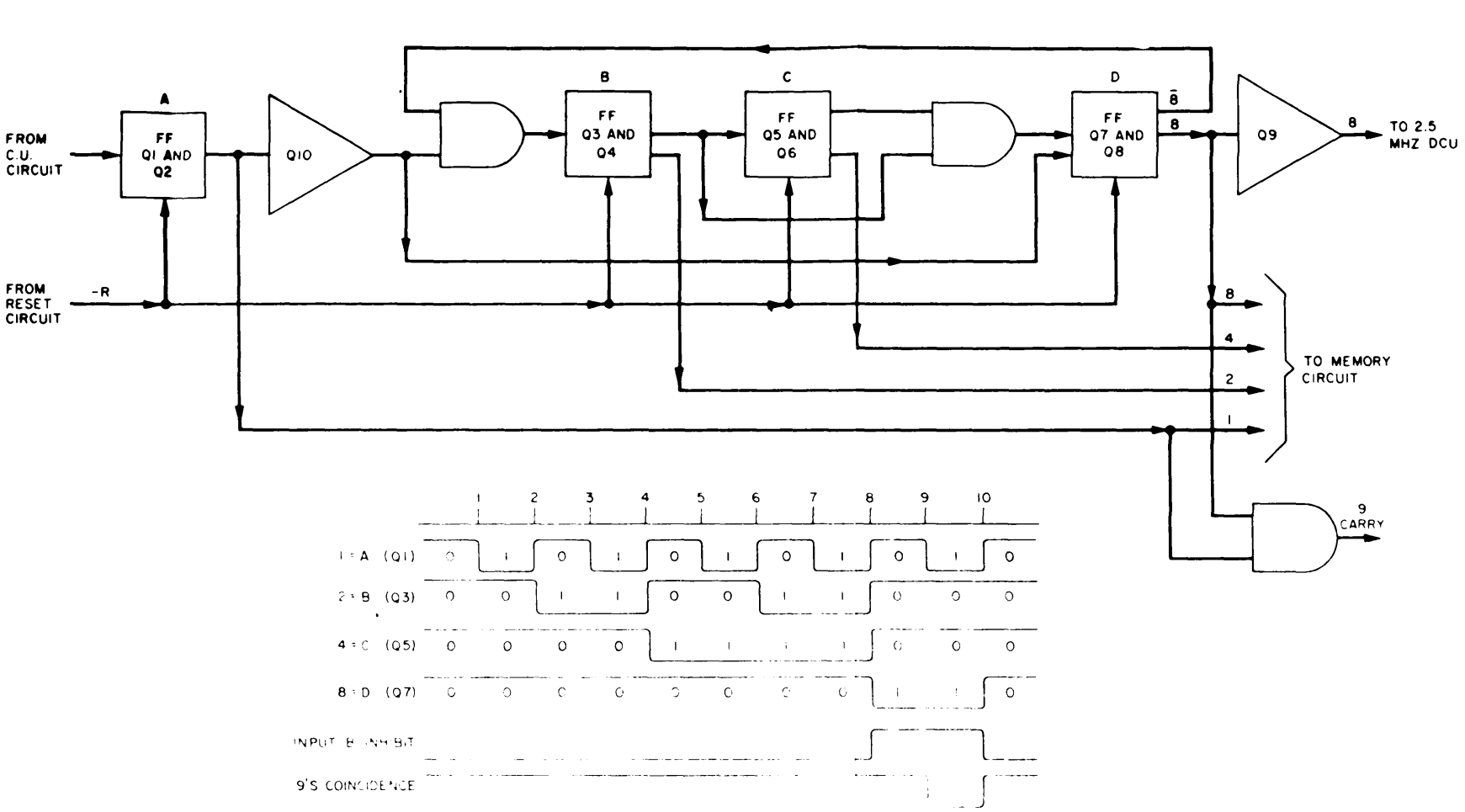


Figure 19. 25-MHz Decade Counting Unit, Block Diagram

The AND gate isolates the third binary output from the fourth binary input after the fourth binary is set. After the tenth pulse is received, the desired final output pulse is produced by a gating-ahead pulse applied to the fourth binary (1 stage) by the first binary. The setting of the fourth binary Inhibits the AND gate between the first and second binaries, and enables the nine-carry AND gate. The ninth pulse is applied to the nine-carry AND gate and an output is produced. Since the AND gate between the first and second binaries is inhibited, the tenth pulse output from the first binary is fed-ahead to the fourth binary (D stage) to reset it. The fourth binary, resets to produce the tenth pulse which also results in all the binaries returning to zero. A carry pulse is thus transferred through amplifier Q9 which acts as input trigger to the next stage. Resetting the 25-MHz decade counting unit to aero is similar to the resetting to zero function discussed for decade counters in Paragraph 20 Q (4). Electrical readout is obtained in a similar manner as discussed for decade counters in Paragraph 20 o (6). Refer to memory readout circuit, Paragraph k for decimal display function details.

h. 2.5-MHz Decade Counting Unit Circuit, (A13, A38, A40, A41, A42, A43, and A44). The 2.5-MHz decade counting unit circuit serves as a decade counter in the counting circuit or in the time base generator circuit. Operation is similar to that described for the 25-MHz decade counting unit discussed in Paragraph 29 g. A noted exception is the removal of Q10, the emitter follower stage and the third binary (not the first) setting the fourth binary. There is no display array connected to the binaries when used in the time base generator circuit. A block diagram of the decade counting unit is shown in Figure 20 and circuit timing is shown in Figure 21. A decade counting unit is an arrangement of four cascaded binaries (flip-flop) that generates one output pulse for every ten input pulses. Consequently, when a frequency is applied to the input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return to its original state). The resultant output of the first binary is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The desired division by ten is obtained by gating in front of the second binary. The tenth pulse provides the desired final output pulse. When used in the time base generator, the nine-carry output pulse is applied to a common ninecarry line with the other decade counting units. After all the decade time base counting units contain a coincident nine-carry, an output pulse will occur from the decade counting unit circuit. The nine-carry pulse serves to trigger the start-stop flip-flop in the ratio and control circuit. On the tenth input a carry pulse is transferred through Q09 to the following stages. Resetting the decade counting unit to zero is similar to the resetting to zero function discussed for the decade counters in Paragraph 20 o (4). Electrical readout is obtained in a similar manner as discussed for the decade counters in Paragraph 20 o (6). Refer to memory readout circuit, Paragraph k for decimal display function detail.

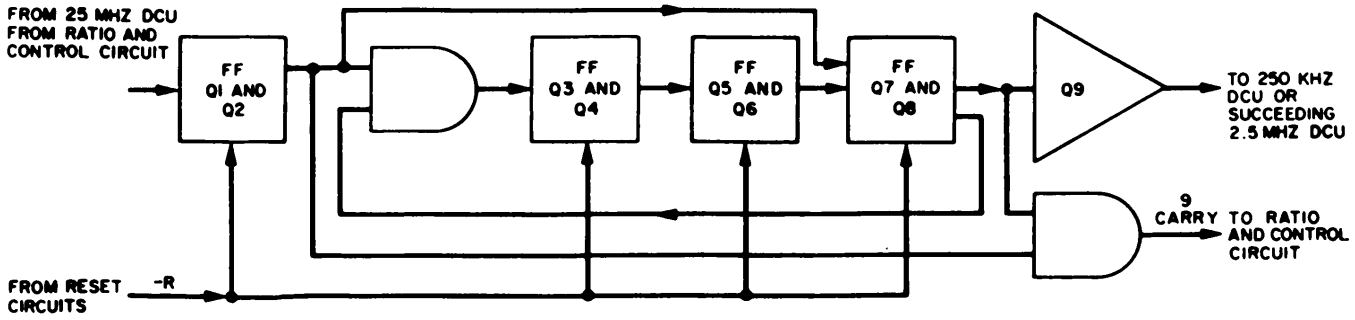


Figure 20. 2-5-MHz Decade Counting Unit, Block Diagram

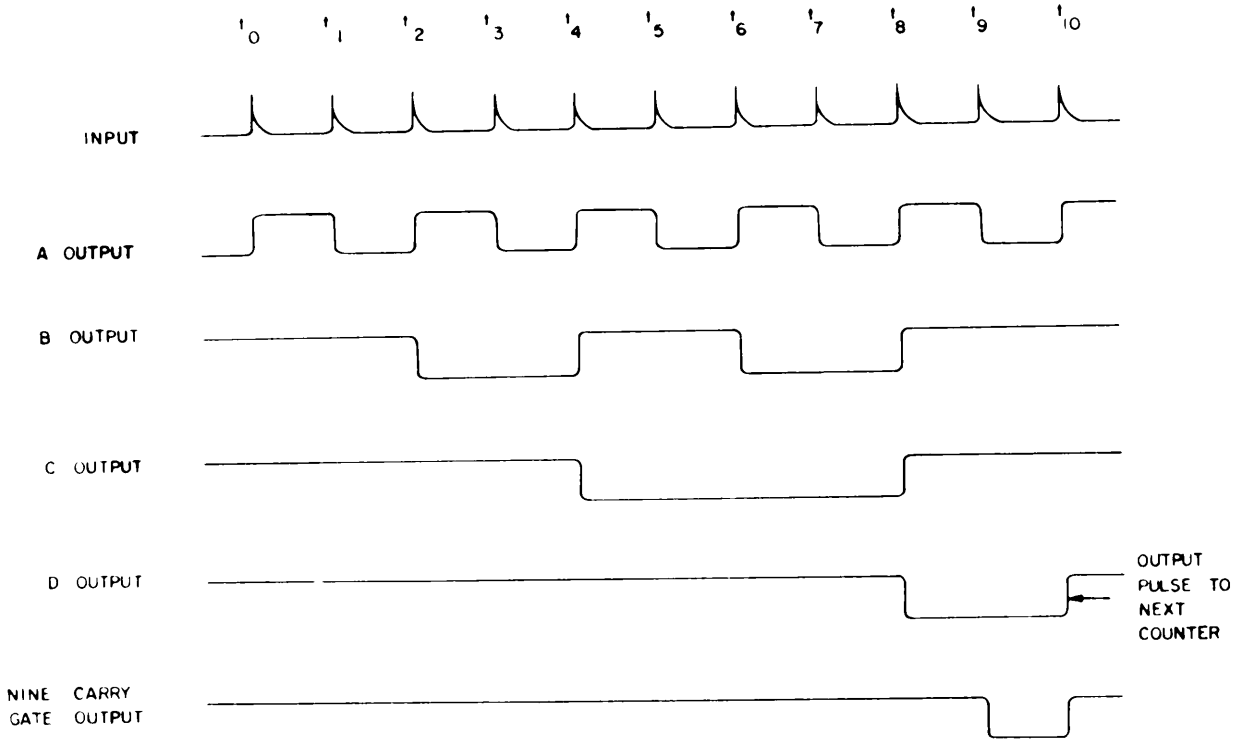


Figure 21. 2.5-MHz and 250-KHz Decade Counting Units, Timing Functions

i. 250-KHz Decade Counting Unit Circuit (A15, A17, A19, A21, A39). The 250-KHz decade counting unit circuit serves as a decade counter in the counting circuit or in the time base generator circuit. Operation and timing is similar to that described for the 2.5- MHz decade counting unit discussed in Paragraph 30g. A noted exception is the removal of carry amplifier Q9. There is no display array connected to the binaries when used in the time base generator circuit. A block diagram of the decade counting unit is shown in figure 22. A decade counting unit is an arrangement of four cascaded binaries (flip-flop) that generates one output pulse for every ten input pulses. Consequently, when a frequency is applied to the input, the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant output of the first binary is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The desired division by ten is obtained by gating in front of the second binary. When used in the time base generator the nine-carry output pulse is applied to a common nine-carry line with the other decade counting units. After all the decade time base counting units contain a coincident nine-carry, an output pulse will occur from the decade counting unit circuit. The nine-carry pulse serves to trigger the start-start-stop flip-flop in the ration and control circuit. Resetting to zero is similar to resetting to zero function discussed in the decade counting unit in Paragraph 20o(4). Electrical readout is obtained in a similar manner as discussed for the decade counting unit in Paragraph 20 o (6). Refer to memory readout circuit, Paragraph k for decimal display function details.

j. Matrix Circuit (A7). The matrix circuit amplifies and decodes the output from the C.U. circuit. The decoded 8421 binary output functions are then applied to the memory readout circuit flip-flop to be further decoded. A block diagram of the matrix circuit is shown in Figure 23 and circuit timing functions is shown in Figure 24.

(1) Quinary Input. The C.U. circuit, which divides the input frequency being measured by 10 provides a quinary electrical readout of the accumulated count stored in the binaries. Since the memory readout circuits functions with a binary 8 input, the quinary 5 output from C.U. circuit requires further decoding (converting) to a usable code.

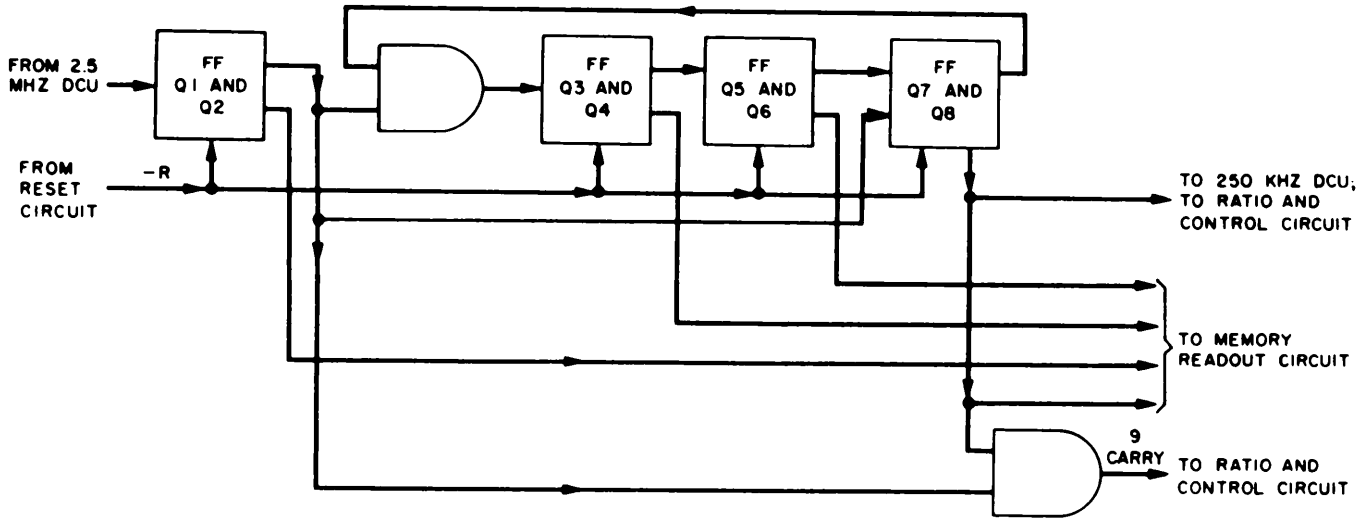


Figure 22. 250-KHz Decade Counting Unit, Block Diagram

(2) Matrix Operation. Amplifiers Q10 through Q17 amplify the matrix circuit quinary input levels and then apply them to the decoding matrix circuits to generate the binary 8 output. Five functions (A = 0, B = 1, C = 0, D= 1 and E = 0) are supplied from the C.U. circuit. The matrix circuit is designed to cause the input levels to revert to a normal state if an input level is absent; that is, a flip-flop remains in the state to which it was set, while a differential amplifier will revert back to its original state when the input level is absent. The differential amplifier will revert back to its original state due to a constant bias level on one half of the amplifier circuit which will cause conduction in the associated transistor. Since the differential amplifier outputs from the matrix circuit are applied to flip-flops in the memory readout circuit, the reverting action back to in original state, will also cause the generation of a reset pulse to the associated flip-flop.

k. Memory Readout Circuits, (A8, A10, A12, A14, A16, A18, and A20). The memory readout circuits serve to convert the binary weights developed in the decade counting unit or matrix circuit to a decimal value. This value is displayed on the glow-tube readout indicators in a decimal form. A block diagram of the memory readout circuit is shown in Figure 25. Each memory readout circuit contains four flip-flops circuits that are connected to binaries in an associated decade counting unit. The four flip-flops are simultaneously set when the read pulse (supplied from the rest circuit) is applied to the individual memory readout circuits by the display pulse. The resultant state that is set into the four flip-flops is applied to resistor decoding gates. This sets the bias level to the glow-tube driver transistor. The output from the resistor decoding gates is applied to additional decoding gates that drive the individual numerical elements in the glow-tubes.

(1) Read Amplifier. The read amplifier (A8Q19) is normally biased to remain cutoff. The resultant collector output bias voltage developed at the junction of R3 (see fig. 43, memory readout schematic) will be between (10 and zero volts depending on the conduction state of the circuit. The voltage level is used to inhibit the flip-flop in the memory readout circuit from changing states until the read pulse is applied to the memory readout circuit. The bias voltage is applied to the four flip-flop circuits through isolation resistors R6, R11, R14, R19, R22, R27, R30 and R35.

(2) Flip-Flop Inhibiting. The bias voltage developed by the read amplifier, biases the bases of transistors Q1 through Q8 to a level above the emitter bias levels (between +2 to +5 volts). When the read amplifier conducts, the bias level drops to a negative level below zero volts. This bias level enables the input flip-flops to function normally: that is, change their states as determined by the weight of the signal applied to their individual bases.

(3) Flip-Flop Setting. The associated input decade counting unit flip-flop weights, supplied through isolating resistors, are applied to the bases of the flip-flop chain. One weight will be high (0) and the other will be low (1). The high level will be near zero volts and the low level will be near -.9 volts. If the bias level applied to Q1 is high, (zero volts), Q1 will cutoff and Q2 will conduct. The resultant voltage levels developed at the collector of each transistor is applied to the emitters of alternate gates which

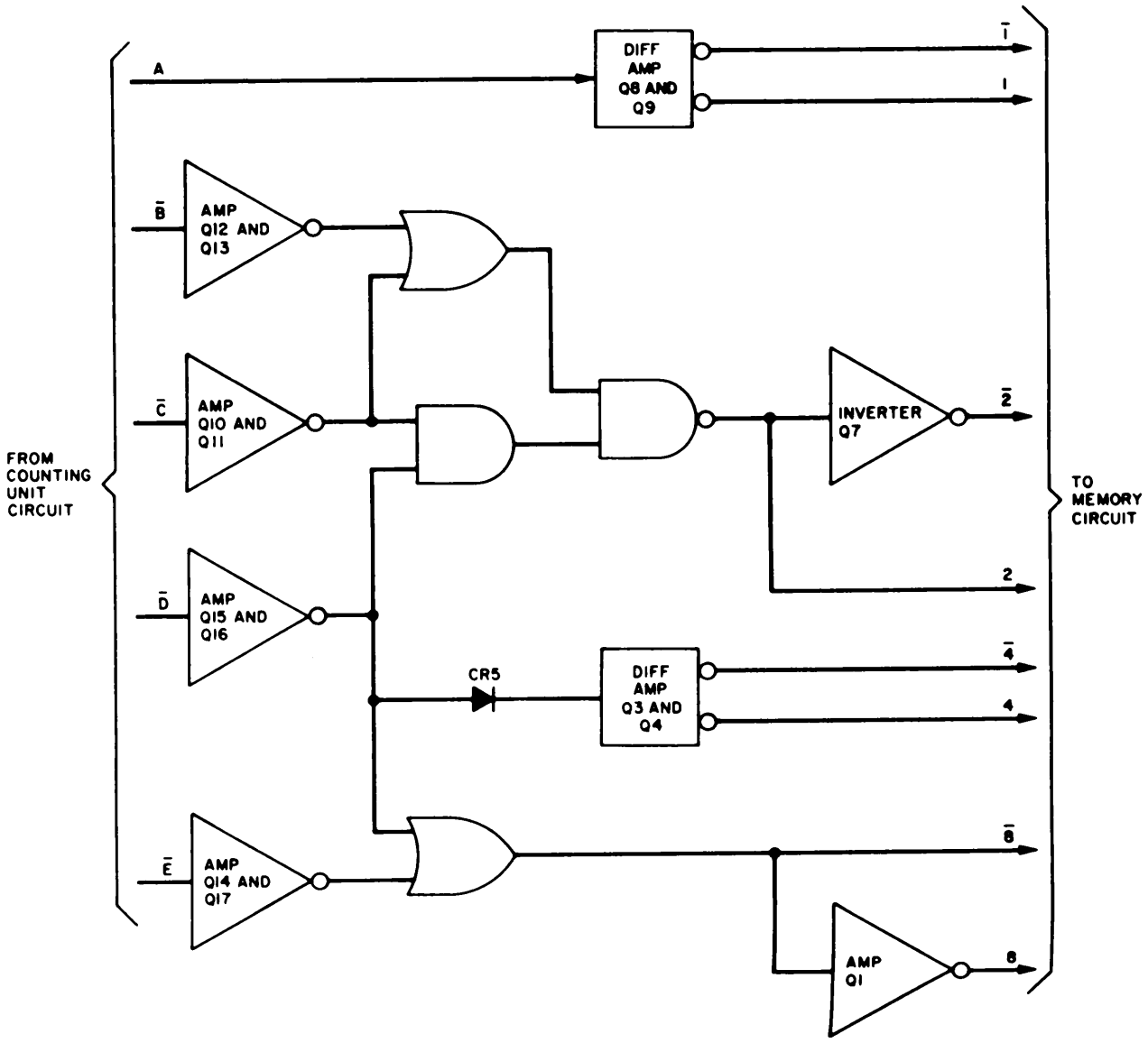


Figure 23. Matrix Circuit, Block Diagram

drive the readout glow tube elements. These two lines determine the odd or even decimal number to be selected.

(4) Numerical Indication Selection. Assume the number 1 is to be illuminated. The BCD code required and applied to the flip-flops will be 0001. Flip-flops Q2, Q3, Q5 and Q7 are required to be in a conductive state. The collector output level at Q1 sets a low condition to the readout glow tubes driving Q10, Q12, Q14, Q16 and Q18. High input levels (1) are applied to decoding gate comprised of resistors R40, R45, and diode CR1. The gate is enabled and produces a high level output. The resistor gate output is applied to the bases of Q9 and Q10 which enables the driving transistors. Since Q1 (the odd line) enables the emitter of Q10, the voltage level causes Q10 to conduct ionizing the numerical indicator.

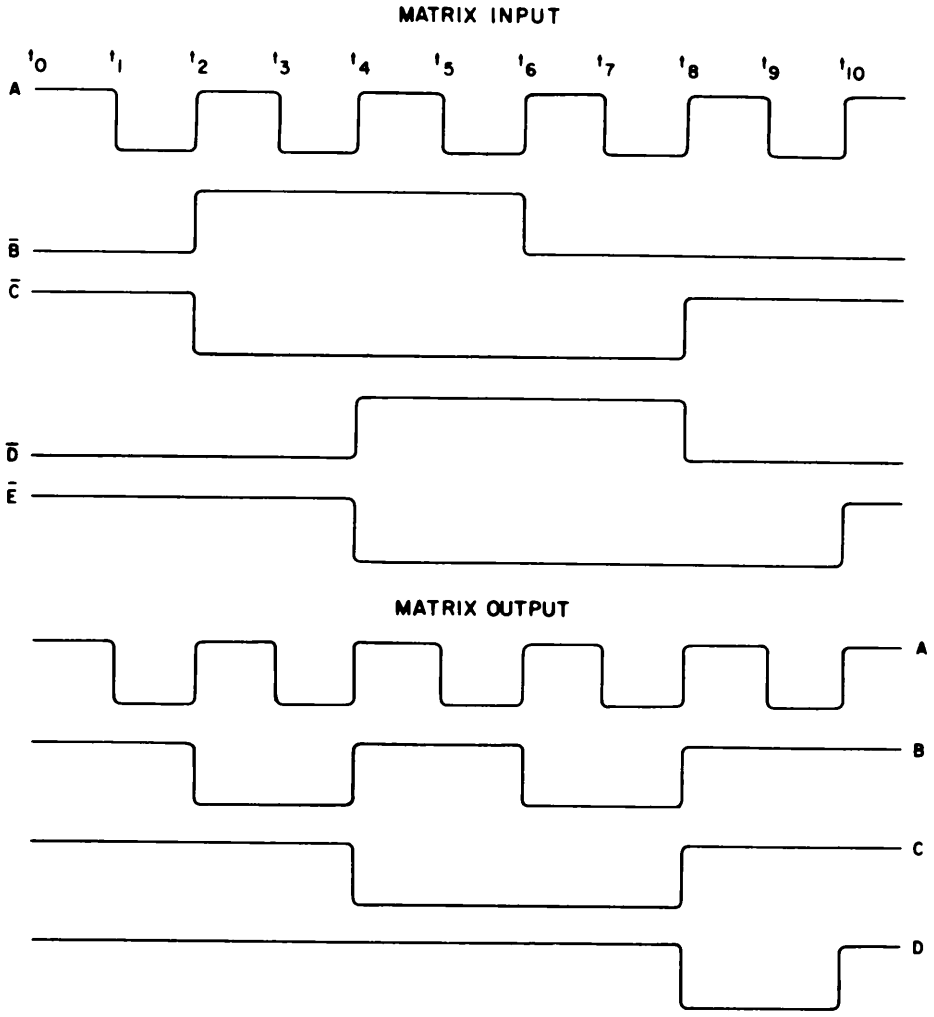


Figure 24. Matrix Circuit, Timing Functions

(5) Numerical Indication Selection Truth Table.

Decimal #	On State Decoding Binaries	On State Numerical Driver	Decoding R's	BCD Input Code 8421
1	Q2-Q3-Q5-Q7	Q10	R40, R45, CR1	0001
2	Q1-Q4-Q5-Q7	Q11	R38, R44	0010
3	Q2-Q4-Q5-Q7	Q12	R38, R44	0011
4	Q1-Q3-Q6-Q7	Q13	R41, R43	0100
5	Q2-Q3-Q6-Q7	Q14	R41, R43	0101
6	Q1-Q4-Q6-Q7	Q15	R39, R42	0110
7	Q2-Q4-Q6-Q7	Q16	R39, R42	0111
8	Q1-Q3-Q5-Q8	Q17	R46	1000
9	Q2-Q3-Q5-Q8	Q18	R46	1001
0/10	Q1-Q3-Q5-Q7	Q 9	R40, R45, CR1	0000

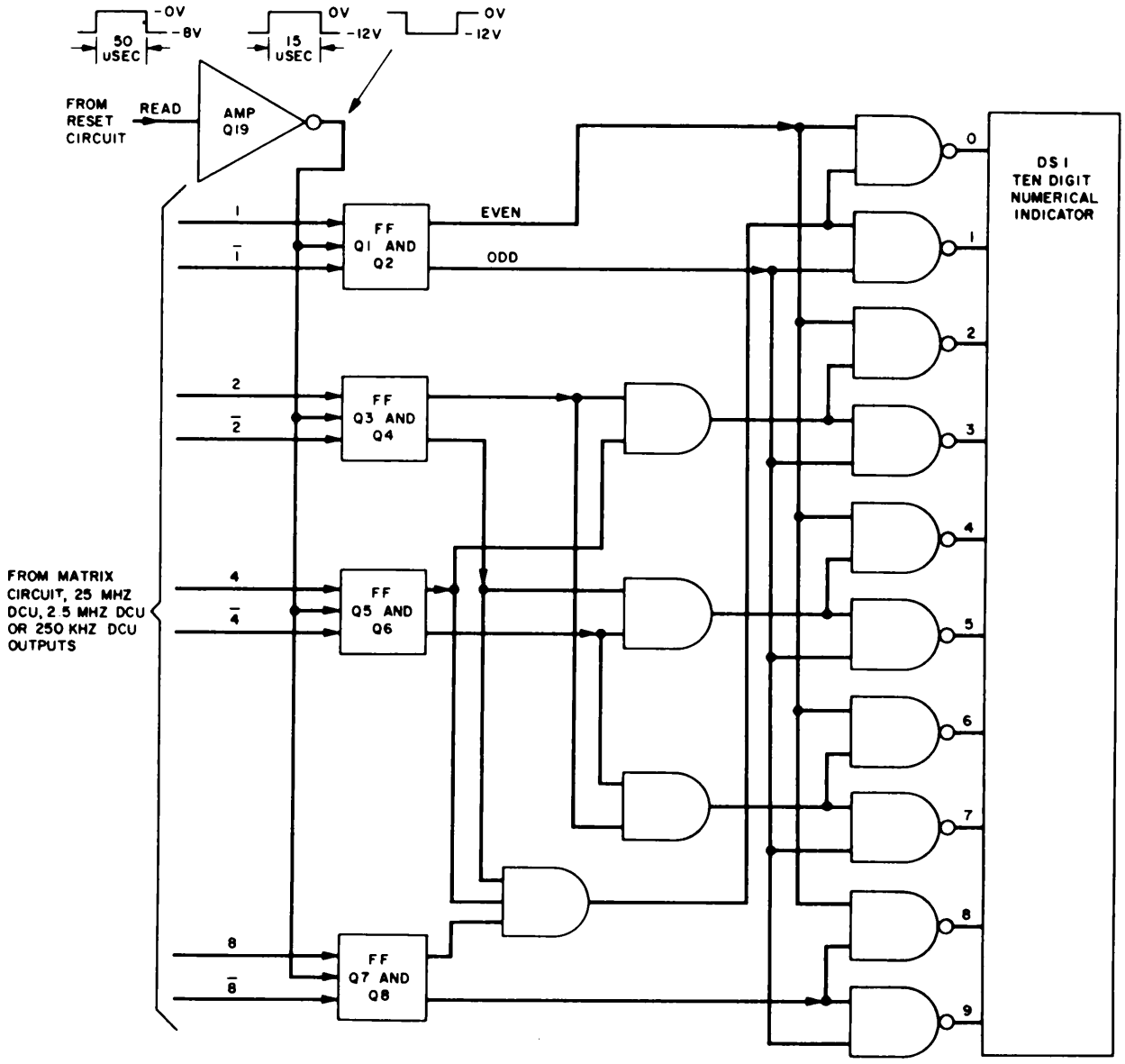


Figure 25. Memory readout, Block Diagram

(6) Readout Glow-Tube. The readout indicator is a cold-cathode type glow-tube containing an inert gas. A positive 330-volts dc is applied through a current limiting resistor to the anode of the tube to excite the gas. When an element gate is enabled, the associated cathode which is connected to ground, causes ionization of the inert gas surrounding the element. The ionization will appear in the numerical shape of one of the ten digits.

(7) Readout Glow-Tube Illumination. Since the number one cathode is in series with Q10 the gas surrounding the number one elements becomes ionized. The element will remain ionized until the four flip-flops are reset (by the read pulse) to display another digit arrangement.

(8) Illumination of Remaining Numbers. The remaining numbers are individually illuminated in a similar manner. The voltage levels set by the flip-flops are applied to resistors R38 through R44 to develop enabling levels to the gates driving the remaining numbers. As the various levels are set by the flip-flops, and the read pulse, the individual gate to the element is enabled.

l. A. D. Circuit, (A29). The A.D. circuit is a trigger generator for the ramp generator input divider circuits. A block diagram of the A.D. circuit is shown in figure 26. The AD circuit will produce a trigger to change the N-Ratio level each time the parity circuits cause an error reset. To impart stability and minimize spurious triggering three such error resets are needed to trigger an output, also the AD circuit is inhibited during display time. The AD circuit consist of a one-shot trigger generator Q7/Q9, gates CR3, 5 & 6 and amplifiers Q5 and Q6.

(1) Error reset pulses applied to Q5, charge intergrating capacitor C11 through gate CR3. Diode CR4 clamps any positive transients that may be present to ground. Gate CR5 is held off by the cut-off state of Q6. Successive error resets will charge C11 until the one-shot Q7/Q8 is brought into conduction. Q7 conducting will partially discharge C 15. Each time the one-shot is triggered the N-Ratio level is stepped to a new value.

(2) During display time the negative going display pulse brings Q6; conduction. Q6 conducting inhibits CR3 and intergrating capacitor C 11 is completely discharged.

(3) Each pulse causes the ramp generator circuit to develop a new N-Ratio as described in Paragraph 41 o. The resultant output from the ramp generator circuit is reapplied to a filter network in the A.D. circuit consisting of resistor R27 and capacitor C 12. The noise levels developed by the ramp generator circuit output are smoothed by the action of the filter network. This develops a smoothed step sawtooth voltage level which is then applied to the I.C. circuit as the N-Ratio level for processing.

Note: Transistor Q1 through Q4 and their associated components are not used in this instrument. No circuit function description will be provided in this manual.

m. Divide-By-16 Counting Unit Circuit, (A:34). The divide-by-16 counting unit circuit serves as a simple frequency divider to provide voltage level inputs to the ramp generator circuit. A block diagram of the divide-by-16 counting unit is shown on Figure 27. The divide-by-16 counting unit circuit is an arrangement of four cascaded binaries (flip-flops) that generates one output pulse for every 16 input pulses from the A.D. circuit. The first binary divides the frequency by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant frequency is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The sixteenth pulse is applied to the divide-b)y-8 counting unit for further division. The four binaries voltage level outputs (weights) are applied to the ramp generator circuit inputs for further processing.

n. Divide-By-8 Counting Unit Circuit, (A: .5). The divide-by-8 counting unit circuit serves as a simple frequency divider to provide voltage level inputs to the ramp generator circuit. A block diagram of the divide-by-S counting unit is shown on Figure 27. Operation is similar to that described for the divide-by-16 counting unit discussed in Paragraph m. In this case the weights of the three binaries are also applied to the ramp generator circuit. The divide-by-8 counting unit circuit is an arrangement of three cascaded binaries (flip-flops) that generates one output pulse for every eight input pulses supplied from the divide-by-16 counting unit circuit. The first binary divides the input by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant frequency is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of eight at the output of the third binary. Therefore, after the eighth pulse is received, the binaries will have returned to the same state following the reset pulse. The three binary voltage level outputs are applied to the ramp generator circuit inputs for further processing. A total of 128 pulses are required to reset the combined binaries (divide-by -16 and divide-by-8 counting unit circuits) to their original states.

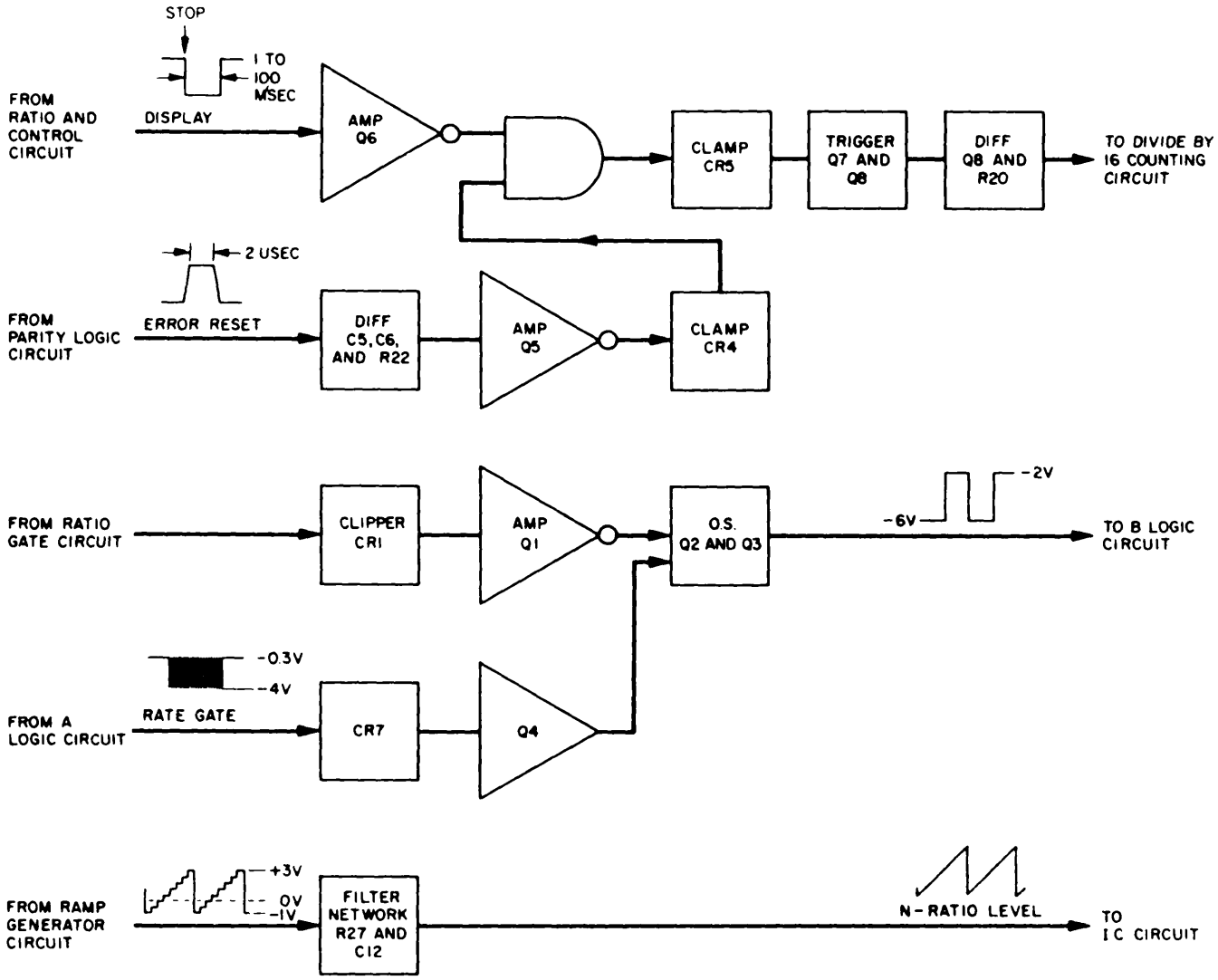


Figure 26. A. D. Circuit, Block Diagram

o. Ramp Generator Circuit, (A33). The ramp generator serves to generate the N-Ratio level voltage applied to the I.C. circuit. A block diagram of the ramp generator circuit is shown on Figure 27. The ramp generator circuit contains seven differential amplifier circuits. The amplifiers are connected in such a manner as to cause the state of an)y of the seven differential amplifier output transistors to affect the final output voltage level from the ramp generator circuit. Each differential amplifier output-transistor-base is connected to the output-transistor-base in the other differential amplifiers. The associated collectors are connected to a common voltage divider summing network. The voltage divider is arranged to connect the collectors of the differential amplifiers in a series arrangement. The differential amplifier input transistor conduction state is determined by the weight of the related flip-flop input supplied from the divide-by-16 or the divide-by-8 counting units. The first differential amplifier (Q13 and Q14) output transistor collector voltage level (which will be high or low depending on whether the transistor is in a nonconduction or a conduction state), is weighed as a binary number and then algebraically summed with the output from the second differential amplifier weight to develop a voltage level that will be between -1 and +3 volts. The states of succeeding differential amplifiers, properly weighed, are also summed. If the outputs from the differential amplifiers transistors are in a conduction state, the transistor collector outputs will be at a low voltage level, and the resultant voltage output level from the ramp generator will be -1 to ± 0.3 volts. If the outputs from the differential amplifier transistors are in a nonconduction state, the transistor collector outputs will be at a high voltage level, and the resultant voltage output level will be +3 +0.3 volts. The voltage level will remain at a final level as long as no additional input pulses from the A.D. circuit are applied to the divide-by- 16 counting unit (causing the counting units to change state. During normal operation, if the input frequency applied to the display indicator changes, the N-Ratio value will also change (due to error reset pulses generated by the parity logic circuit) to maintain the S.C. circuit output between a nine to ten megahertz frequency. If a higher N-Ratio value is required, the parity logic circuit generates an error reset pulse which causes the ramp generator to change the N-Ratio level

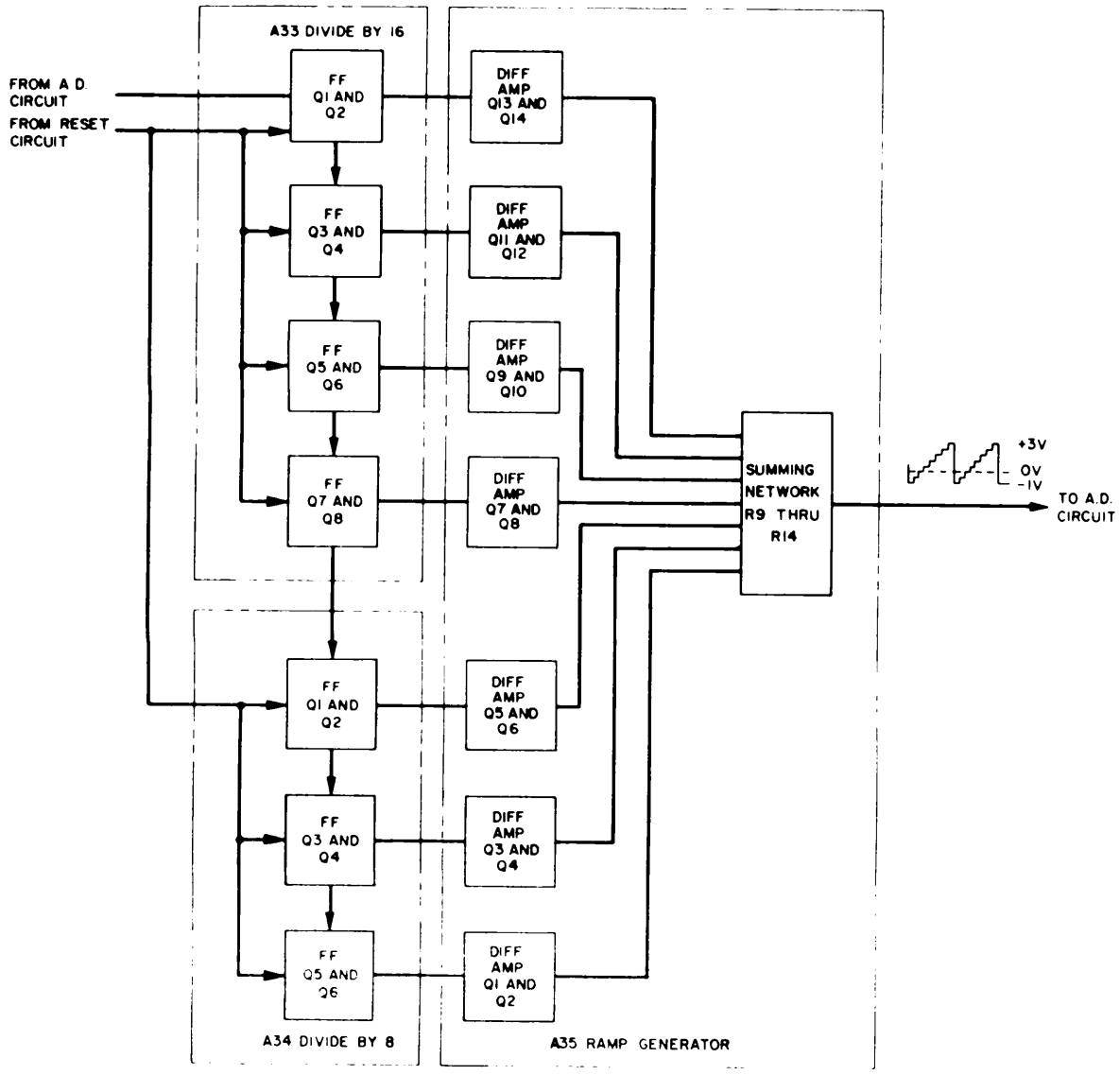


Figure 27. Divide-BY-16, Divide-By-8, and Ramp Generator, Block Diagram

level that is applied to the I. C. circuit. If this level and subsequent higher levels are unsatisfactory, that is, a lower N-Ratio level is required, the parity logic circuit detects this unsatisfactory condition and the ramp generator is caused to recycle through to the lowest level (0) and start generating a new N-Ratio level. The ramp generator circuit output may have several N-Ratio levels that will work for any given frequency. The ramp generator circuit output is applied to the A. D. circuit for filtering and then to the I. C. circuit as the N-Ratio voltage level for further processing.

p. A Logic Circuit, (A25). The A logic circuit serves to divide the f_2 sync frequency (supplied from the F. S. circuit) and to develop the ratio gate pulse applied to the ratio gate circuit. A block diagram of the A logic circuit is shown in Figure 28. Operation of the A logic circuit is similar to that described for the divide-by-16 counting unit, Paragraph m.

(1) The A logic circuit is an arrangement of four cascaded binaries (flip-flops) that generates two output pulses. When the 1.5 KHz sync (slow time base) frequency is applied to the input of the binary, (see fig. 29) the first binary divides it by two (since the first pulse switches the binary to the opposite state and a second pulse is required to return it to its original state). The resultant frequency is again divided by two in the second binary (making a total division by four). This process continues in each binary with an expected total division of sixteen at the output of the fourth binary. The eighth pulse is received and the third binary generates an output pulse which is then applied to the ratio gate circuit as the ratio gate pulse. This pulse develops the burst of 4N signal from the f2N frequency supplied from the I. S. circuit. The resetting of the third binary also serves to set the fourth binary which develops the alternate reset pulse. The alternate reset pulse is applied to the ratio gate flip-flop (A26Q8 and A26Q9) in the parity logic circuit.

(2) During operation the remote operation buffer energizes relays A48K1 and A48K2 to select the proper mode of division. The relays apply disabling voltages to transistors A25Q4 and A25Q6 to prevent a flip-flop action to occur in the circuits. The resultant action causes the second and third binaries to act as emitter followers, resulting in a division by two in the A logic circuit instead of the division by eight.

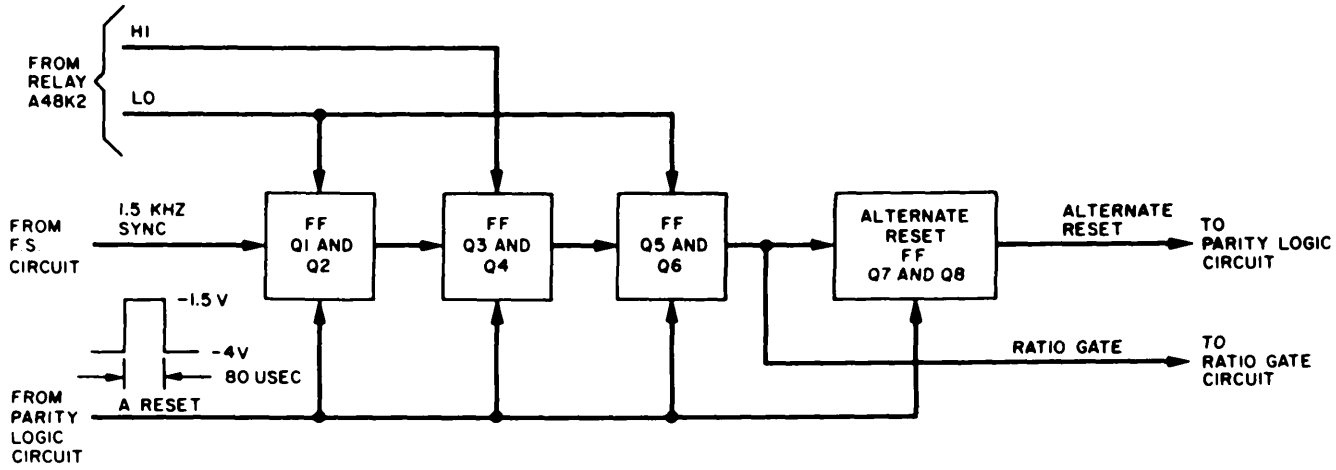


Figure 28. A Logic, Block Diagram

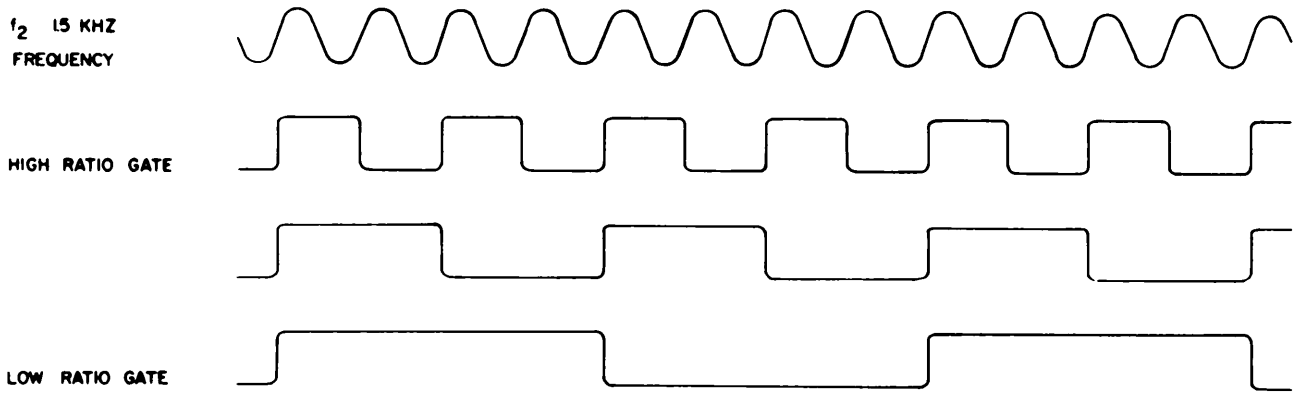


Figure 29. A Logic, Timing Function

g. B Logic Circuit, (A27). The B logic circuit divides the burst-of-4N signal from the ratio gate circuit. It also develops a single-burst-of-N signal. The single-burst-of-N is then applied to the parity logic circuit for further processing. A block diagram of the B logic circuit is shown in Figure 30. Operation of the circuit is similar to that described for the A logic circuit and discussed in Paragraph m. The action of the B logic circuit is to divide-by-four the 4N signal with a resultant single-burst-of-N frequency output generated. The B logic circuit is an arrangement of three cascaded binaries (flip-flops) that generates two output pulses. When the 4N signal is applied to the input, the first binary divides it by two. The resultant frequency is divided again by two in the second binary (making a total division of four), and so on, with an expected total division of eight at the output of the third binary (see fig. 31). After the third input pulse is received, the binaries will be in a state corresponding to a count of three pulses. The fourth pulse resets the first binary. The first binary output resets the second binary. The second binary output is then applied to the parity logic circuit as the single-burst-of-N signal. The third binary develops a check signal (odd-even pulse) which is used to develop the consistency check function in the parity logic circuit. The third binary counts the amount of N present in the burst-of-4N signal twice and the resultant count results in the third binary being reset to its normal state. If the third binary output state results in a set condition, the weight of the binary is applied to the odd-even gate (A26Q3 and A26Q4) in the parity logic circuit as an odd condition. This alerts the computation error check circuit that an inconsistency exists, since the sum of the two identical bursts-of-N signal must be even. The four binaries are reset by the alternate reset pulse (from the A logic circuit) that is delayed 30 microseconds by the 30 microsecond delay gate (A26Q1 and A26Q2) in the parity logic circuit.

r. Parity Logic Circuit, (A26). The parity logic circuit provides the consistency check function of the electronic counter frequency measurement. A block diagram of the parity logic circuit is shown in Figure 32. During normal operation, the burst-of-N signal is applied to the parity logic circuit for checking. If the frequency counter is computing accurately, the burst-of-N signal is allowed to pass through the parity logic circuit and is applied to the ratio and control circuits for further processing. If the parity logic circuit determines that a consistancy error exists, an error reset pulse is generated that is applied to the reset circuit. The error reset pulse causes the resetting of the frequency counter circuits and a new frequency measurement cycle to be generated.

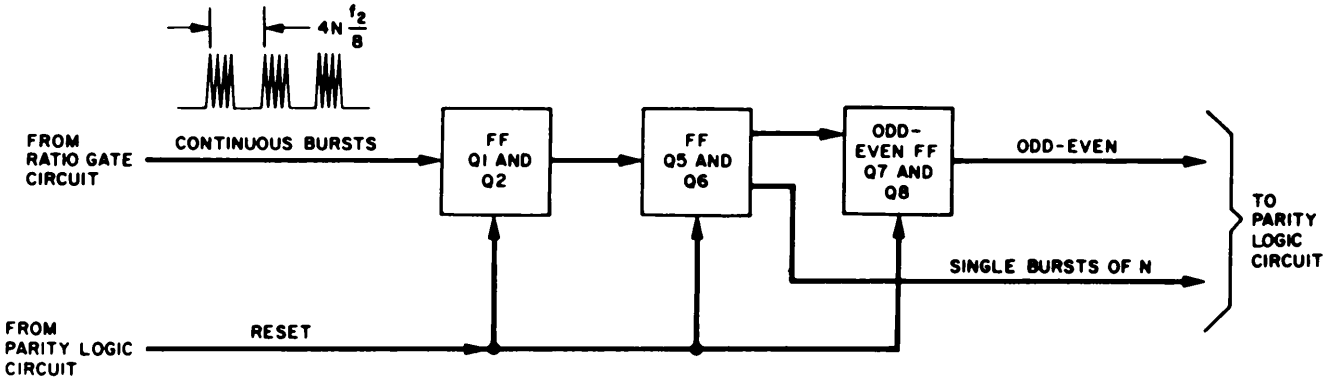


Figure 30. B Logic, Block Diagram

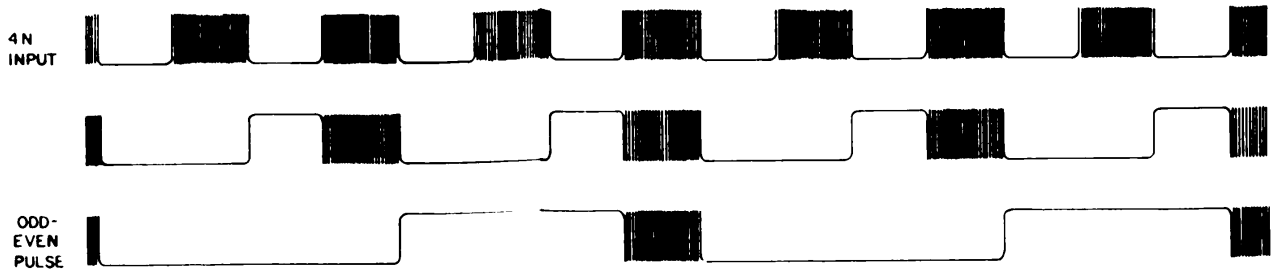


Figure 31. B Logic, Timing Functions

(1) The burst-of-N signal, supplied from the B logic circuit, is applied to AND gate CR9. The ratio gate flip-flop (Q8 and Q9) is also connected to the AND gate. The flip-flop is initially set for (t) at cut off. The alternate reset pulse supplied from the "A" logic circuit is also applied to the ratio gate flip-flop. The alternate reset pulse does not set the ratio gate flip-flop until the alternate reset pulse goes to a reset state. Therefore the first burst-of-N signal will be passed through the AND gate and applied to the ratio and control circuit for further processing.

(2) After the burst-of-N signal is processed in the ratio and control circuit, the signal is applied to two ratio decade counters (A38 and A39). The NOT function from the second binary in the first decade counter (A38) is returned to the greater-than-four flip-flop (A26Q10 and A26Q11). The greater-than-four flip-flop is initially set for Q10 at cutoff. The burst-of-N signal is divided once more while still in the B logic circuit to develop the odd-even pulses. The odd-even pulse is applied to OR gate Q3: with the greater-than-four pulse from the decade counter. If the generated odd(l-even pulse ends in an odd condition, or the greater-than-four flip-flop output is less than four, the OR gate generates an output pulse. This pulse is applied to an AND gate along with the parity enable pulse.

(3) The parity enable pulse is generated by the 80 microsecond one-shot flip-flop (transistors (.5 and Q6). Initially transistor Q6 is biased conducting. As the reset pulse occurs, transistor Q6 is cutoff and the 80 microsecond pulse is generated. 'The transistor Q6 output is coupled to transistor Q5 through resistor R14. Transistor Q5 now conducts causing the collector voltage level to drop to a low level and discharging capacitor C9 through transistor Q5. The resultant voltage change generates a pulse that is coupled to AND gate Q4 through resistor R10 and diode CR12, along with the 30 microsecond delay pulse.

(4) The alternate reset pulse applied to the ratio gate flip-flop is also applied to the 30 microsecond delay pulse generator circuit Q2. The alternate reset pulse is differentiated by capacitor C1 and resistor R1, limited by diode CR1, and applied to the base of transistor Q2. Transistor Q2 is normally biased conducting. The alternate reset pulse cuts off transistor Q2. This causes a current change through resistor R8. Two pulses are generated at the collector of Q2. The pulses applied through capacitor C4 to clamp diode CR4 and AND gate diodes (CR3, and CR5) as a 30 microsecond delay pulse. The pulse is ANDed with the parity enable pulse from transistor Q6 and the output is applied to AND gate Q4. The 30 microsecond pulse is also applied to the B logic circuit as a reset pulse for the B logic circuit binaries.

(5) If an output is generated by OR gate Q3, this pulse is ANDed with the output from CR3 and CR5 AND gate. The resultant pulse generated is applied to OR gate Q7. The output pulse generated from transistor Q7 becomes the error reset pulse. The pulse is applied to the reset circuit and causes an interruption of a frequency computation if a consistency error exists.

s. Ratio and Control Circuit, (A37). The ratio and control circuit amplifies and shapes the 1-,MHz crystal oscillator output into square pulses, develops the N-Ratio measurement, and generates the N-Timing gate -pulse. A block diagram of the ratio and control circuit is shown in Figure ;33.

(1) The 1-MHz signal is applied to the 1-MHz shaper circuit (Q1 and Q2) to develop the 1-MHz square pulses. The pulses are applied to three decade dividers (A40, A41, and A42) and gates (Q2, Q4 and CR12). The 1-MHz signal is divided by 1000 in the three decade dividers to develop a 1-KHz pulse which is reapplied through OR gate Q4 to two additional decade dividers (A43; and A44).

(2) The nine-carry output from decade (dividers A40 through A44 is applied to the nine-carry line input to the start-stop flip-flop circuits and provides the trigger pulse to the start flip-flop (A37Q8 and A37Q9).

(3) The one-burst-of-N input from the parity logic circuit is supplied to the OR gate Q3 with the 1-MHz pulses. Diode CR12 is enabled by the readout flip-flop (Q6 and Q7) to pass the 1-MHz pulses to gate Q4.

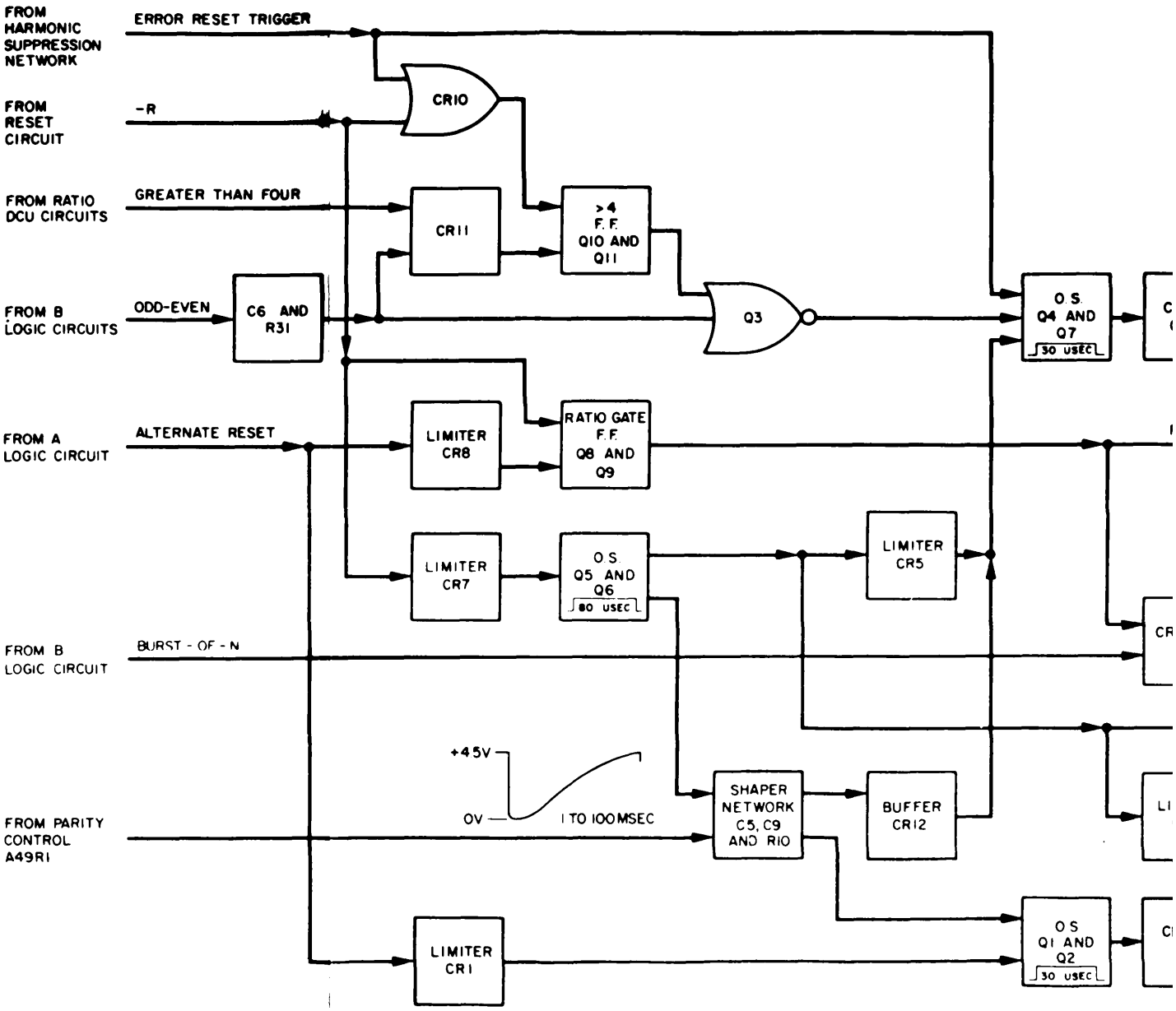


Figure 32. Parity Logic, Block Diagram

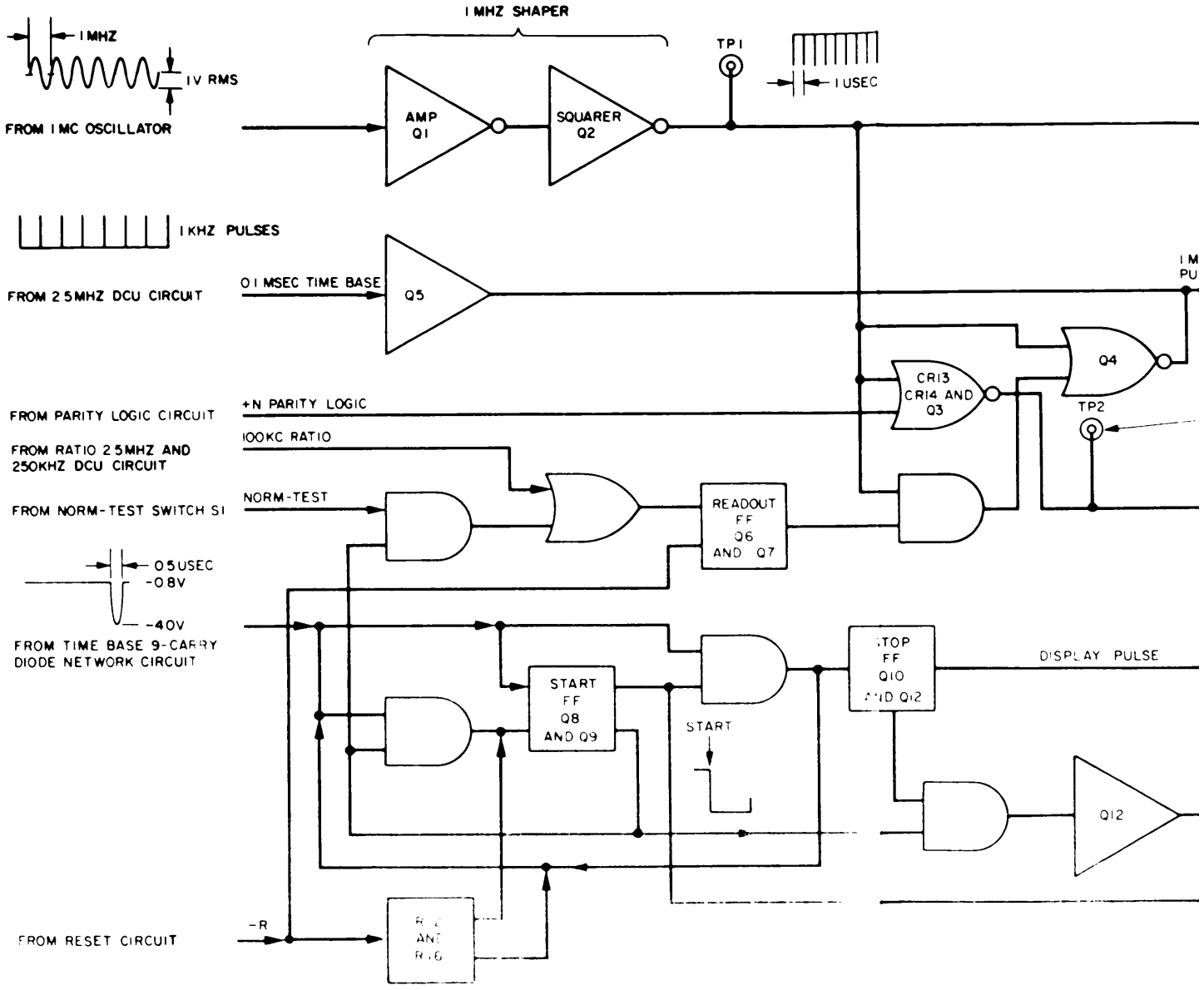


Figure 33. Ration and Control, Block Diagram

(4) After the reset pulse occurs, the readout flip-flop is set so that transistor Q7 is conducting. The read-out flip-flop is enabled and decade dividers A38 through A44 are cleared. The resultant high level at the collector of A37Q7 is applied to diodes CR12 and CR13 to inhibit their conduction. This action prevents the 1-MHz pulses from passing through the gates. The burst-of-N pulses are applied to the ratio decade dividers (A38 and A39). An error count is developed and applied to the readout flip-flop. As the reset pulse clears all circuits, the A40, A41, and A42 decade dividers commence dividing the 1-MHz pulses. The ratio decade dividers output (A38 and A39), is then applied to the readout flip-flop to enable gates A37Q4 and A37CR12. The resultant action allows a certain amount of 1-MHz pulses to pass through gate Q3 into decade divider A43 and A44 between the 1-KHz pulses. Since decade dividers A43 and A44 are normally counting 1-KHz pulses, the 1-MHz pulses are made-to occur between two 1-KHz pulses. This action sets a count into the two decade dividers so the final countinterval is speeded up; that is, shortened.

(5) As additional 1-KHz pulses are counted, the second nine-carry pulse is generated at a time interval that is related to the one-burst-of-N pulse. The second nine-carry pulse sets the stop flip-flop to end the N-Timing gate pulse interval. The first nine-carry pulse occurs from decade dividers A40, A41, A42, A43, and A44, and sets the start flip-flop and generation of the N-Timing gate pulse. The set pulse will occur approximately after the reset pulse occurs. The nine-carry pulse passes through AND gate A37 CR4 and sets the start flip-flop QB. The output AND gate CR6 and CR7 is inhibited until the start flip-flop is set, also enabling diode CR7. The resultant resetting of Q9 inhibits AND gate CR4 but also enables AND gate CR5. As the second nine-carry pulse is generated by decade dividers A43 and A44, the stop flip-flop is set, thereby inhibiting diode A37CR6 in the output AND gate. This setting of the start-stop flip-flops and resultant enabling and inhibiting of the output AND gate causes the generation of the N-Timing gate pulse. The N-Timing gate pulse is then applied to the C. U. circuit input through emitter follower Q12.

t. Reset Circuit, (A36). The reset circuit generates reset pulses, a read pulse applied to the memory readout circuits, and the print command pulses required to operate an external mechanical printer.

A block diagram timing chart of the reset circuit is shown in Figure 34. The reset circuit consists of three individual circuit functions controlled by a unijunction one-shot multivibrator circuit. These three are the display timer generator, the reset pulse one-shot generator and the read pulse one-shot generator. Operation of the display timer provides the primary trigger control to the reset and read one-shot multivibrators. Since all control functions are initially set by the reset pulse, the pulse is required to initiate the frequency measurement sequence.

The timing chart shows the time relationship of the following action. The nine-carry pulses (generated by the time base generator circuits) initiate the start-stop flip-flop action. At stop time a negative going display pulse is generated (by the stop flip-flop A37-Q10 and Q12) as shown in Figure 34. The leading edge of the display pulse initiates the resulting read, reset, and print commands.

(1) Display Timer Circuits. The display timer circuit, consisting of transistors Q1 through Q4, provide the timing control for each frequency measurement in the display indicator. The operation of a unijunction transistor (Q3) provides the timing cycle that originates the trigger pulses applied to the reset one-shot multivibrator. The generation of the reset pulse is initiated by the application of the display pulse to transistor Q1. Transistors Q1 and Q2 form a trigger circuit and provide print command trigger pulses to an external mechanical printer. It also provides trigger pulses to the read one-shot multivibrator. Transistor Q1 is normally conducting. With Q1 on, Q3 is held off and the parallel timing capacitors C4 and C5 are in a neutral state (no charge). The negative going transition of the display pulse sets the trigger circuit Q1/Q2 by cutting off Q1. By reversing the conduction states of Q1 and Q2 the positive and negative print command pulses are generated in the respective collector circuits. Q2 provides a negative going print command and Q1 a positive. This positive. This positive signal from Q1 allows the timer capacitors (C4 and C5) to charge. This charge time is primarily the RC time of C4/C5 and R24. An expotential voltage rise will be felt at the emitter of Q3. Also applied to the emitter are synchronizing pulses applied through Q4 from the F. S. circuit. The combined influence of the positive charge on C4/C5 and the sync pulses will bring Q3 into conduction. With the conduction of Q3 the capacitors C4/C5 are discharged and the negative going transition ends the display cycle. This results in a reset signal causing an end to the display pulse enabling the trigger circuit Qi/Q2, returning Q1 to the ON state, thus preventing Q3 from acting like a free running oscillator.

(2) Reset One-Shot. The reset one-shot multivibrator is normally biased with transistor Q7 off. The pulse supplied from transistor Q3 through capacitor C10 is a negative-going trigger pulse. This pulse drives Q7 into conduction for the duration of the r-c time constant of capacitor C11 and resistor R31. The positive going 20 microsecond pulse, applied to the base of transistor Q9 by voltage divider resistors R32 and R33, is used to develop a negative going pulse at the collector of Q9. This pulse is applied as a negative going reset pulse throughout the instrument. A positive reset pulse is taken directly off the collector of Q7 and applied as required throughout the instrument.

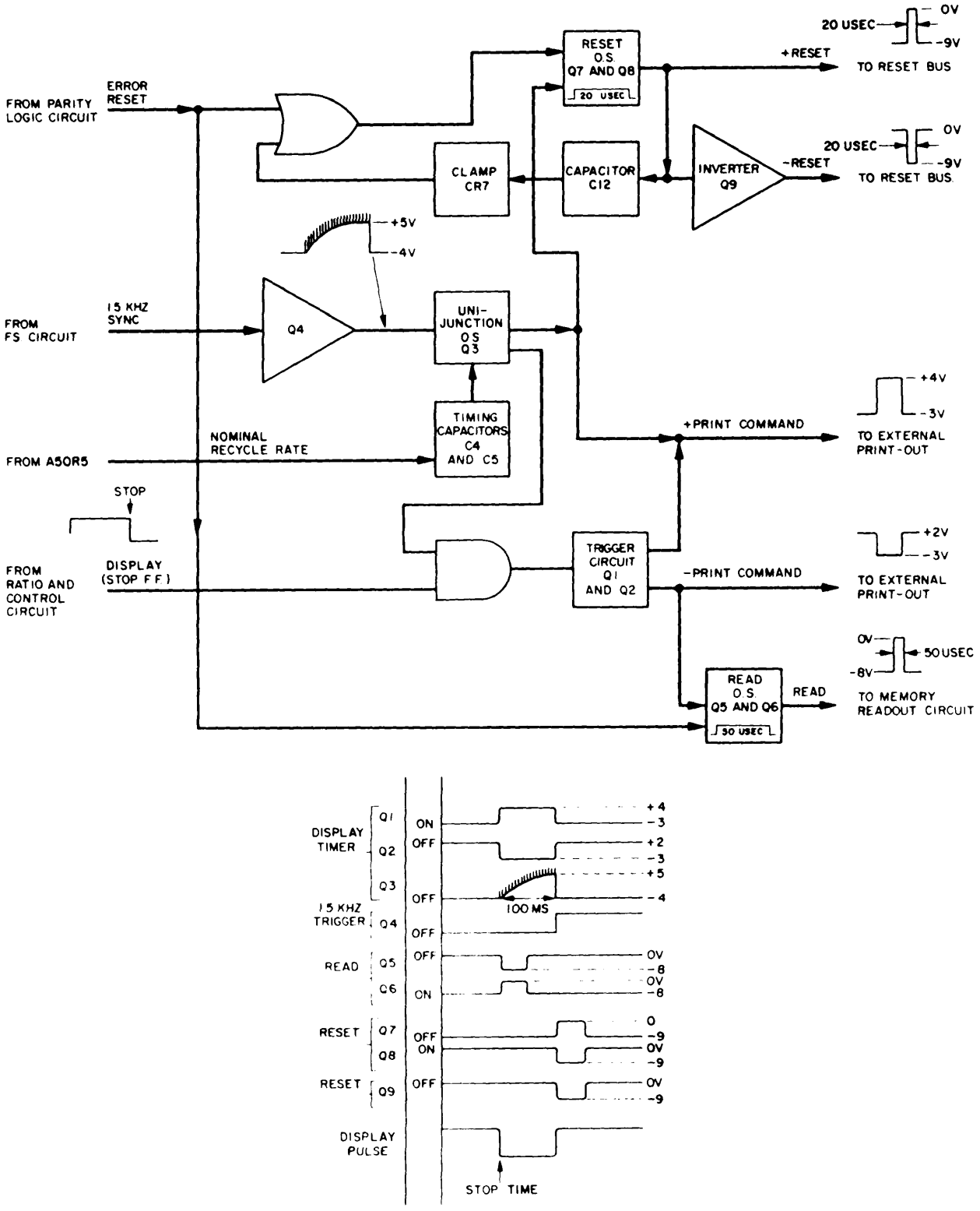


Figure 34. Reset Circuit, Block Diagram

(3) Secondary Reset Control. The reset one-shot may also be set by trigger pulses supplied through OR gates diodes CR6, CR8, CR9, and CR10. Capacitors C14, C16, and C17 that provide the inputs to the Oil gates are biased to charge when one side of any one capacitor is grounded. The charging action of the capacitor causes a positive output pulse to be generated from the OR gate. The OR gate output is applied to the base of transistor Q8. Transistor Q6 is biased to conduct and the OR gate output causes the transistor to cutoff. The collector output from Q8 is coupled to the base of transistor Q7 through capacitor C11 and resistor R31. As transistor Q8 cuts off transistor Q7 conducts for the duration of the r-c time constant of C11 and R31. This results in the generation of the reset pulses.

(4) Read Pulse One-Shot. The read pulse applied to the memory readout circuits is generated by the read one-shot transistors Q6 and Q6. As the display pulse causes transistor Q1 to cutoff, Q2 comes into conduction. The voltage change in transistor Q2 collector output is applied to the read one-shot multivibrator through capacitor C18 as a negative going trigger pulse. Transistor Q6 is normally biased conducting. The negative going trigger pulse causes the transistor to cutoff. The transistor is cutoff for the duration of the r-c time constant developed by capacitor C2 and resistors R5 and R7. This generates a 50 microsecond pulse. The pulse is then applied to the read amplifiers in the memory readout circuits (and the display indicator readout decoder circuits) to transfer the totalized N-Count set into the memory readout flip-flops.

(5) Read Pulse Secondary Control. The read one-shot may also be triggered by the error reset pulse generated in the parity logic circuit. The positive-going error reset pulse, is coupled to the read one-shot multivibrator through capacitor C1 and buffer diode CR1. Transistor Q5 is biased at cutoff and the error reset pulse causes the transistor to conduct for the duration of the read pulse as described above.

(6) Print-Command Pulse Output. The print command pulses (+ and -) are generated by the display timer trigger circuit, Q1 and Q2. The two amplifiers are in a normal quiescent state (Q1 conducting and Q2 cutoff). Application of the display pulse to the base of QI causes Q1 to cutoff and results in the generation of the print command pulses. The two collector outputs of the differential amplifier are applied to an external mechanical printer-readout through the PRINT-OUT connector J22. The print command signals actuates the printer circuits when readout information is available.

u. Remote Operation Buffer Circuit. (A4)). The remote operation buffer circuit serves to 1) generate the enabling gate signal supplied to the preset generator circuits, and 2) energizes relays A48K1 or A48K2 and the coaxial switch A48A1S1 as necessary to provide the proper circuit control functions that determine the offset frequency compensation to be used within the electronic counter. A block diagram of the remote operation buffer circuit is shown in figure 5. When the associated receiver operation band is selected, the receiver automatically supplies a program control signal (+12 to +28 volts dc) to the remote operation buffer circuit input. The voltage is processed and applied to the individual circuit or combination of circuits to accomplish the function desired as listed in table 6.

(1) Band I Program Control. A program control voltage applied to pin K of connector J3 is amplified by transistors A45Q1 and A45Q2. The resulting positive voltage level change at the collector of transistor Q2 is applied to the -21.40 MHz preset generator (A22) input AND gate. This same voltage change is also applied to coaxial switch driver transistor Q13 and to relay A48K1 OR gate A45CR7. The voltage level energizes relay A48K1, provides an enabling voltage to the preset generator circuit input, and causes transistor A45Q13 to conduct. Transistor Q13 is normally biased at cutoff. Positive 12 volts dc is applied to the collector of Q13 through the coaxial switch solenoid and therefore the switch is deenergized. The conduction of Q13 will energize the coaxial switch. The switch now selects the low frequency input to the electronic counter. Removal of the applied voltage causes the circuit to return to a normal state inhibiting transistor Q13 and de-energizing the solenoid.

Table 6. Preset Frequency Truth Table

Using Band	Manufacture Band	Input Jack	Coaxial Switch A48A1S1	Relay A48K1	Relay A48K2	Input Frequency Range	Readout Frequency Indication
I	A	J1	X	X		1 KHz to 120 MHz	9987.600
II	B	J1	X			81.4 MHz to 300 MHz	9978.600
III	C	J2				295 MHz to 560 MHz	9940.000
IV	D	J2			X	550MHz to 1.06 GHz	9940.000
V	E	J2			X	1 GHz to 2.5 GHz	0000.000 (Not Used)

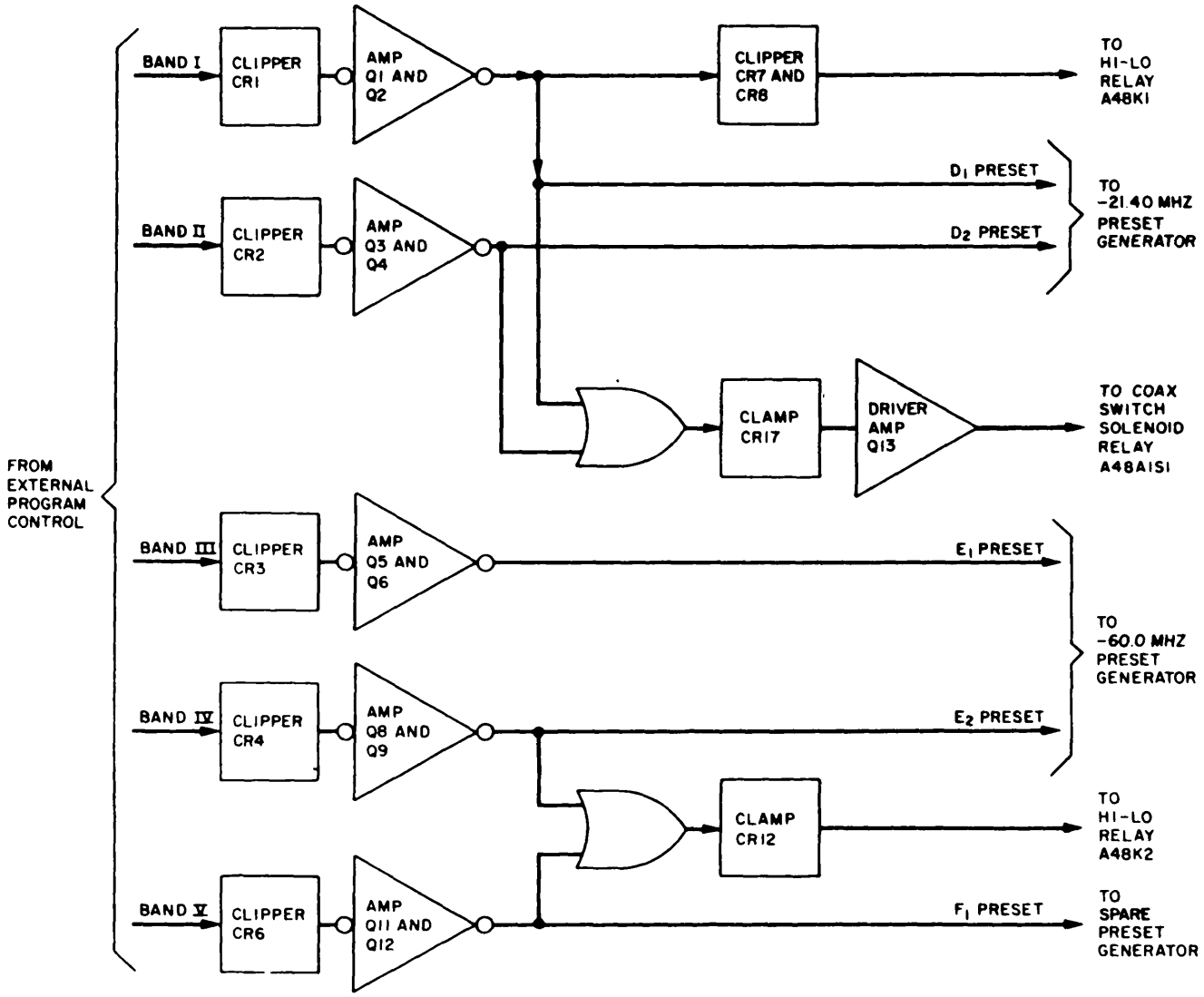


Figure 35. Remote Operation Buffer, Block Diagram

(2) Band II Program Control. Relay control in Band II is similar to Band I control except relay A48K1, which is not required in Band If, is not energized. The program control voltage is applied to pin L of connector J3 and amplified by transistors A45Q3 and A45Q4. The voltage level change at the collector of transistor Q2 is also applied to the -21.40 MHz preset generator input AND gate and to the coaxial switch driver transistor Q13, through OR gate CR14. The OR gate CR13 is back biased to ground by transistor Q2 collector load resistor R7. Diode CR1:3 isolates the input to transistor Q13 from relay A48K1. The voltage level change at transistor A45Q4 provides an enabling voltage to the preset generator AND gate and also causes transistor Q13 to conduct. Transistor Q13 then functions as described for Band I selecting the low frequency input for the electronic counter.

(3) Band III Program Control. As listed in Table 6, the three program control relays are in a deenergized condition in Band III. A program control voltage applied to pin M of connector J3 will only provide an enabling signal to the -60.0 MHz preset generator (A23) input gate. The signal is amplified by transistors A45Q6 and A45Q7 and applied directly to preset generator A23 input AND gate, as an enabling signal.

(4) Band IV and V Program Control. Program control in Band IV and V energizes relay A48K2 through OR gate CR9 and CR11 and also enables preset generators A23, or A46. The program control voltage is applied to pins N (Band IV) or P (Band V) of connector J. It is then amplified by transistors A45Q8 and A45Q9 (Band IV) or A45Q12 (Band V) and applied to relay OR gate. The output of amplifiers Q8 and Q9 is applied to preset generator A23 as an enabling signal while the output from amplifiers Q11 and Q12 is applied to preset generator A46 as an enabling signal. The selecting of Band IV or V provides the necessary receiver intermediate frequency offset desired and the necessary control signals through the relay to the electronic counter circuits.

v. Preset Generator Circuits, (A22, A23, and A46). The preset generator circuit generates the preset pulse that presets the decade counters to a predetermined count. A block diagram of the preset generator circuit is shown in Figure 36. During normal operation, the intermediate frequency offset control signal is applied to the remote operation buffer circuit which then selects the preset generator circuit to be used (-21.4 MHz, -60.0 MHz, or -160.0 MHz). The remote operation buffer circuit output is applied to preset generator circuit input enabling AND gate CR1, CR2, or CR3. The. reset pulse input is differentiated by capacitor C1, resistors R1 and R2, clipped by diodes CR4 and CR6, clamped by diode CR7. and the resultant pulse is amplified by transistor Q1. This results in a trigger pulse to one-shot flip-flop Q2 and Q3. The pulse is then applied to diodes CR1-A through CR20-A and CR1-B through CR4-B to the decade counting units. The pulse sets the weights of specific flip-flops in the decade counting units. Only specific diodes are installed on the individual preset generator circuit board (as detailed on the schematic) to cause the setting of a specific decimal count.

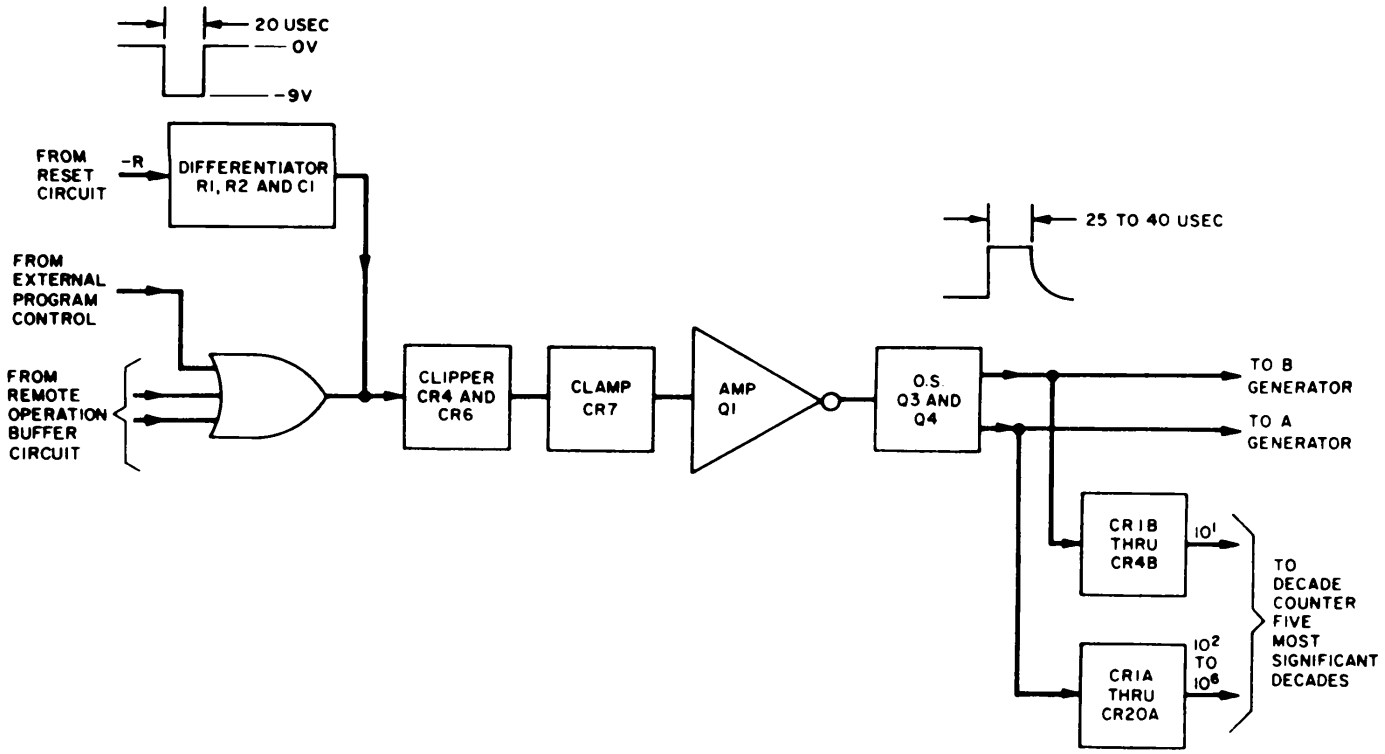


Figure 36. Preset Carrier, Block Diagram

w. Power Supply Circuit, (A47). The power supply circuit provides all the regulated and unregulated voltages use' by the electronic counter and the display indicator. The power supply circuit develops the regulated +12 and ±4.5-volts dc, the regulated +30-volts dc, and the unregulated +330-volt de voltages required by the equipment. The power supply circuit chassis also is the mounting chassis for the power supply regulator printed circuit board connector and the chassis interconnection wiring. A block diagram of the power supply circuit with the associated power supply regulator is shown in Figure 37. The input ac power is supplied to the power supply circuit by setting the POWER SWITCH (A48S1) to ON. Any voltage transients in the power line are filtered by the line filter (A49FL1). The filtered ac power is then applied to the primary winding of transformer A-47T1. Four secondary winding outputs are used to develop the de voltage outputs.

Caution:

Do not apply power to the power supply chassis if the power supply regulator is removed as damage to the instrument circuits may result.

(1) The ac output from a secondary winding is applied through a half-wave rectifier diode CR13 and filter network (C5, R44, and R45) to provide the unregulated +330-volt dc voltage. The +:330-volts dc is then applied to the memory readout circuit to provide anode voltages for the glow tube readouts.

(2) Another output from the secondary winding is applied through the fullwave rectifier diodes (CR13 and CR15) and the filter network (R-17 and C4A) to the power supply regulator circuit. The +:38-volt dc output is regulated in the power supply regulator to develop the regulated +:30-volts dc.

(3) The regulated ±12 volt dc voltages are developed from a third secondary winding output and applied to full-wave rectifier diodes CR6, CR16 (+12 vdc), CR7, and CR8 (-12 vdc). The +18-volt de output from diodes CR6 and CR16 is filtered by capacitor C3B and resistor R39. The filtered +18-volts dc is applied to the collector of series regulator Q13 in the power supply regulator circuits. The +12-volt regulator circuits provides the regulation control current to the base of regulator Q2:. The regulated +12-volt dc output at transistor Q3 emitter is applied through fuse F4 to circuits in the display indicator and also reapplied to the power supply regulator as the reference voltage for the ±12 and ±4.5 volt dc voltage regulator circuits. The -18-volts dc output from diodes CR7 and CR8 is filtered by capacitor C2 and R46 and applied to the collector of series regulator Q1. The -12-volt dc output at the emitter of the regulator is reapplied to the -12-volt regulator circuit as a reference voltage and through fuse F3 to circuits in the electronic counter.

(4) The regulated ±4.5-volt dc voltages are developed from a fourth secondary winding output and applied to full-wave rectifier diodes CR9, CR10 (+4.5 vdc) CR11, and CR12 (-4.5vdc). The +8-volt de output from diodes CR9 and CR10 is filtered by capacitor C3A and resistor R11 and applied to the collector of series regulator Q1 in the power supply regulator circuit. The regulated +4.5-volt de output at regulator Q4 emitter is reapplied to the regulator as the output reference voltage for the +4.5-voltage regulator and through fuse F2 to circuits in the electronic counter. The -8-volt dc output from diodes CR11 and CR12 is filtered by capacitor C1 and resistor R42 and applied to the collector of series regulator Q2. The -4.5-volt regulator in the power supply regulator provides the regulation control for regulator Q2. The regulated -4.5-volt dc output at regulator (Q2 emitter is reapplied to the power supply regulator -4.5-volt regulator circuit as a reference voltage and through fuse F1 to circuits in the electronic counter.

x. Power Supply Regulator Circuits. (A47A1). The power supply regulator circuits provide the +30, ±12 and ±4.5 voltage regulation controlling functions for the dc power supply. A block diagram of the power supply regulator circuits is shown in Figure 37. The power supply regulator is mounted on the power supply chassis.

(1) The unregulated +:38-volts dc supplied by the power supply is applied to the collector of series regulator Q5, to the base of the regulator and to the anode of 30-volt reference diode through resistor R50. The voltage level at the junction of the resistor and diode serves as a voltage reference to prevent the voltage applied to the base of the regulator from rising above 30 volts. If the emitter output from the regulator drops lower than 30-volts, the regulator increases conduction to readjust the emitter output to 30-volts dc. The 30-volt dc output at he regulator emitter is filtered by capacitor C15 and applied to the printed circuit board connector and to the +12-volt dc regulator circuit.

(2) The unregulated +18 volts dc supplied by the power supply to the +12-volt series regulator is also applied to the collector of regulator driver Q4. The regulated output from the series regulator is reapplied to the power supply regulator across voltage divider resistors R19, R20, and R21. Resistor R19 is a low resistance value and paralleled with +12 ADJ control R4. Any voltage change in the voltage divider network is also reflected across the +12 ADJ control which is direct coupled to the base of the error reference amplifier Q2. Transistor Q2 is emitter-to-emitter coupled to reference amplifier Q1 to form a differential amplifier circuit. Any change in current flow in either half of the differential amplifier will be reflected in the other half of the circuit. The error reference amplifier collector output is direct-coupled through current amplifiers Q3 and regulator driver Q4 to the base of series regulator Q3 in the power supply. Since diode CR2 will retain the reference amplifier base at a

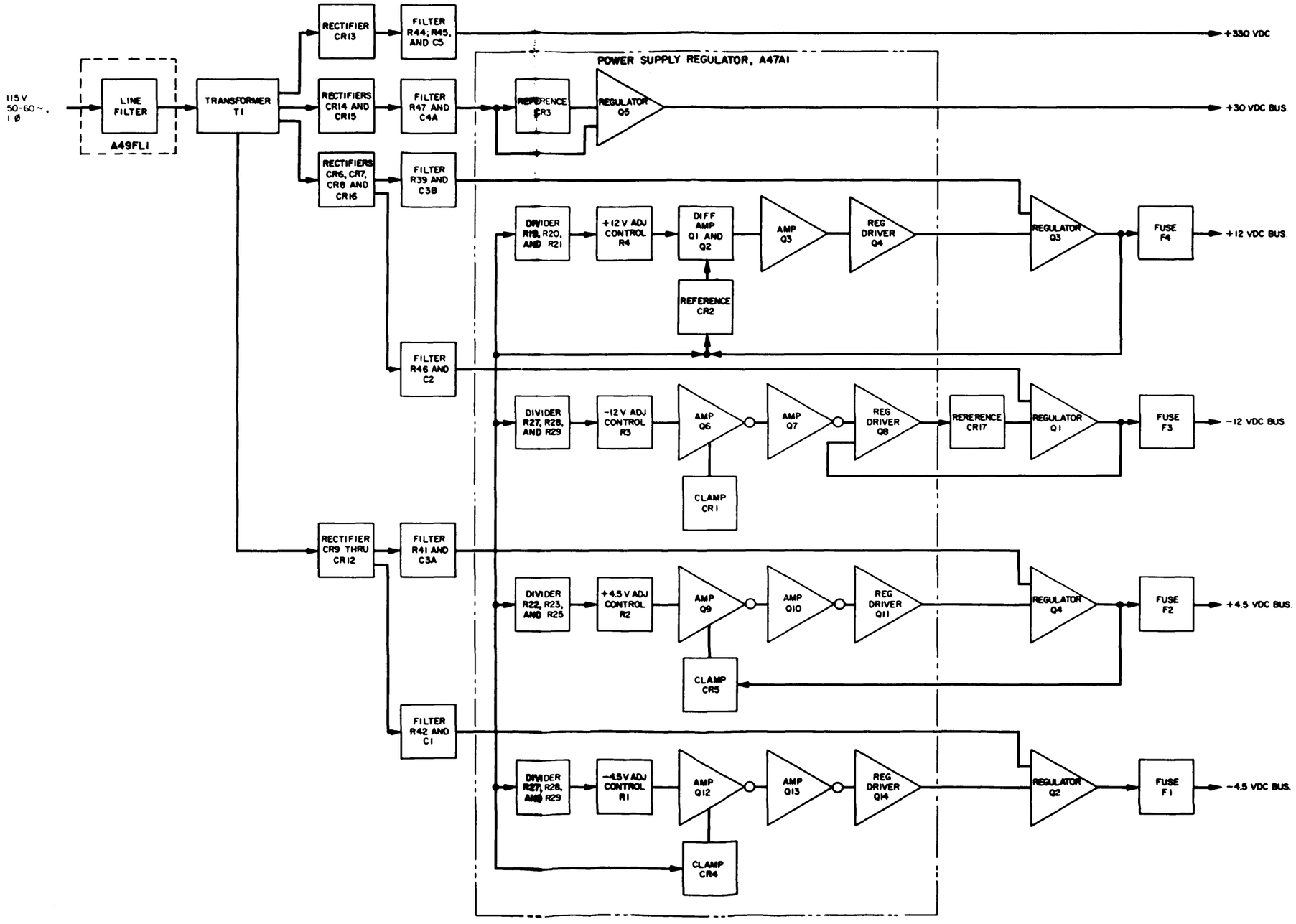


Figure 37. Power Supply Assembly, Block Diagram

constant voltage level. (5.1 volts), any change of the voltage applied to the collector or any change in the voltage drop across the voltage divider network, causes a resultant readjustment in conduction of the series regulator output.

(3) The regulated -12-volt dc circuit functions in a similar manner as the +12-volt circuit. The regulated +12-volts dc is applied across -12 ADJ voltage divider R7, R8, and R14. The -12 ADJ control is paralleled across R8 to permit a fine adjustment of any voltage drop in the voltage divider network. The -12 ADJ control output is amplified by error amplifier Q6 and applied to the series regulator A47Q1 in the power supply through amplifier Q7 and regulator driver Q8. Any change in the voltage drop across the voltage divider network causes a resultant readjustment in conduction of the series regulator to change the regulator emitter output.

(4) The 4.5-volt de regulator circuits are similar to the -12-volt dc regulator circuit and functions in a similar manner. The error reference voltage developed in a voltage divider and the +4.5 ADJ and -4.5 ADJ controls outputs are amplified and applied to series regulators in the power supply. The resultant change in the series regulator outputs is fedback to the individual voltage divider network which results in correcting the regulator output.

y. One-Megahertz Oscillator Circuit. (A47Y1). The 1-MHz oscillator circuit generates a stable one megahertz frequency that serves as the time base generator circuit reference source for all frequency measurements. The oscillator assembly is a thermally insulated chamber which contains a heating element, a temperature sensing circuit, an extremely stable one megahertz piezo-electric crystal, and the associated oscillator circuit components. The -MHz oscillator output is applied to the ratio and control circuit where amplifying and shaping (A37Q1 and A37Q2) is performed to supply one microsecond pulses to the time base generator circuits for scaling and trigger control. Provisions are made to bypass the internal oscillator output and permit the use of an external one megahertz oscillator frequency.

z. Display Indicator. (A51). The display indicator repeats the electronic counter readout frequency indications at a remote location. A block diagram of the display indicator shown in figure 38. The binary output functions for the display indicator are supplied by the decade counter circuits in the electronic counter through a 100-foot interconnection cable assembly.

(1) The display indicator contains seven decoder readout printed circuit boards (A1 through A7) connected to seven in-line glow-tube readout indicators. Flip-flop circuits serve to convert the binary weights (developed in the electronic counter counting circuits) to a decimal value and to display this value (representing the frequency count) on the glow-tube readout indicators in a decimal form. The decoder readout circuits function in a similar manner as the memory readout circuit except that a differential amplifier (Q20 through Q27) drives each flip-flop circuit (Q1 through Q8). The flip-flop states are applied to resistor decoding gates and then to 10 AND gates. Each gate drives an individual numerical element in the glow-tube. The first flip-flop (Q1 and Q2) determines whether the numerical value to be displayed will be an odd number or an even number.

(2) A read pulse is supplied from the display indicator to read amplifier Q19. The amplifier is normally biased at cutoff. The collector voltage level (developed across R:3 and R-4 voltage divider) is applied to the four differential amplifiers as an enabling pulse. The input binary-coded-decimal weights applied to the differential amplifier input transistors will have no affect on the state of the amplifiers until the read impulse causes the read amplifier to conduct. The conduction of the read amplifier (Q19) enables the differential amplifiers. The amplifiers then transfer their states to the flip-flops which are then decoded into a decimal display.

(3) The readout indicator is a cold-cathode type glow-tube with an inert gas in the tube. A positive 330-volt dc voltage is applied to the anode of the tube (through a current limiter resistor) to excite the gas. When an element gate is enabled, the associated cathode is connected to ground, causing ionization of the inert gas surrounding the element. The ionization glow will be in a numerical shape of one of the ten digits in the tube. The individual element will remain ionized until the four flip-flops are reset for another digit arrangement.

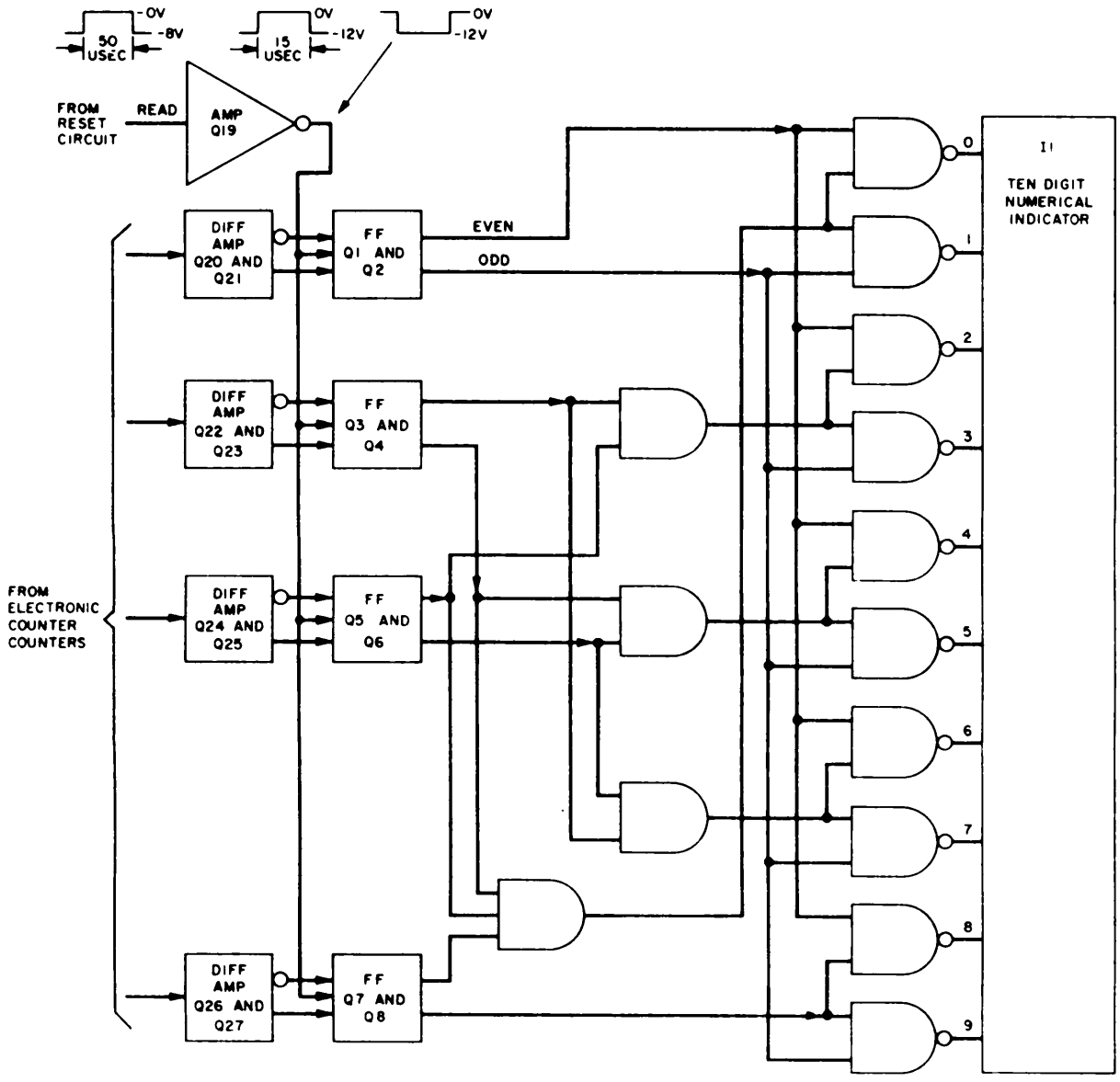


Figure 38. Display Indicator, Block Diagram

CHAPTER 5

MAINTENANCE

Section I. PREVENTIVE MAINTENANCE

32. General

This section provides maintenance and troubleshooting information for the electronic counter. Included are periodic preventive maintenance checks, a performance checkout procedure, troubleshooting procedures, and repair and adjustment procedures.

33. Preventive Maintenance

Preventive Maintenance is the systematic care, servicing, and inspection of equipment to prevent the occurance of trouble, to reduce down time, and to assure that the equipment is serviceable. The preventive maintenance checks and services charts outline checks and services to be performed at a specific interval. These checks and services are to maintain electronic equipment in a service are to maintain electronic equipment in a serviceable condition. To assist operators in maintaining serviceability, the charts indicates what to check, how to check, and what the normal conditions are. The References column in the table lists the illustrations. If the defect cannot be remidied by performing the corrective action indicated, higher echelon maintenance or repair is required.

34. Preventive Maintenance Checks and Services Periods

Preventive Maintenance Checks and Services of the electronic counter are required daily, weekly, monthly, and quarterly.

a. Daily Preventive Maintenance Checks. The Daily Preventive Maintenance Checks are listed in Table 7.

b. Weekly Preventive Maintenance Checks. The Weekly Preventive Maintenance Checks are listed in Table 8.

c. Monthly Preventive Maintenance Checks. The Monthly Preventive Maintenance Checks are listed in Table 10.

35. Cleaning of the Electronic Counter

Caution: Solvents may damage)paint and identification marks.

Equipment may be cleaned by using prescribed procedures utilizing brusher, lint-free cloth, or be vacuuming or by blowing with low pressure air. Specified solvents may be brushed when required for additional cleaning action. The following materials, or their equivalent, are used for maintenance.

Lint-free cloth

Stiff (non-metallic) bristle brush

Solvent (Trichloroethane, Federal Specification O-T-620

Compressed air (filtered, moisture-,and oil-free, : 30 psi maximum) (;0/40

60/40 Solder (Military Specification MIL-S-6872)

Warning: When using solvents provide adequate ventilation and skin protection.

Caution: Solvents may damage paint and identification marks.

Note: Frequent cleansing of the air filter element may be required when the instrument is operated is operated in unusually severe environments.

36. Lubrication Instructions

No lubrication is required.

37. Touchup Painting Instructions

Remove rust and corrosion from metal surfaces by liglitly sanding them with fine sandpaper. Brush two thin coats of paint on the base metal to protect it from further corrosion, Refer to applicable cleaning and refinishing practices specified in Th19-213, Paninting Instructions for field use.

Table 7. Daily Preventive Maintenance Checks and Services Chart

Sequence No.	Item	Procedure
1	Equipment	See that the equipment is complete
2	Connectors	Check the tightness of all connectors. Check connectors for damaged kegways or shells, correct mating alignment, corroded contacts, burns caused by arcing, cracked or dirty insulation material, damaged pins or contacts, and loose or missing attaching parts.
3	Indicator lenses	Check all indicator lenses for cracks.
4	Controls and indicators	While making the operating checks, observe that the mechanical action of each switch is smooth and free of external or internal binding and no excessive looseness is apparent.
5	Blower	Blower should be operating. Blower should cause free air passage through equipment. If blower is operating but air passage is blocked, check air filter as directed in Table 7.

Table 8. Weekly Preventive Maintenance Checks an(l Services Chart

Sequence No.	Item	Procedure
1	Cables	Inspect cords, cables, and wired for (chafed, cracked, or frayed insulation. Replace connectors that are broken arced, or worn excessively.
2	Handle	Inspect handles for looseness - Replace- or tighten as necessary.
3	Metal surfaces	Inspect exposed metal surfaces for rust and corrosion. Clean and touch up paint as required. (Refer to paragraph :3;).
4	Air filter	Inspect air filter on blower fan assembly. No dirt or corrosion should be evident. If air passage is blocked through air filter or if dirt is evident, clean as directed in paragraph :35,.

Sequence No.	Item	Procedure
1	Pluckout items	Inspect pluckout item seating. Make certain that 1 MHz oscillator base clamp grips base securely.
2	Relays	Inspect the relays for dirt, corrosion, and burned contacts.
3	Jacks	Inspect jacks for snug fit and good contact
4	Transformer	Inspect the leads on the power transformer. All mounting nuts must be tight. No dirt, corrosion or oil should be evident.
5	Terminal blocks	Inspect terminal blocks for loose connec tions and cracked or broken insulation.

Table 10. Quarterly Preventive Maintenance Checks and Services Chart

Sequence No.	Item	Procedure	References
1	Publications	See that all publications are complete, servicable, and current.	
2	Modifications	Check to determine if new applicable MWO's have been published. All URGENT MW's must be applied immediately. All NORMAL MWO's must be scheduled.	TM38-750 and USASA Circular 310-11(c)
3	Spare parts	Check all spare parts (operator and organizational) for general condition and method of storage. No overstock should be evident and all shortages must be on valid requisitions	Chapter 9

Section II. PERFORMANCE CHECKS

38. General

This section contains procedures for performance checks of the electronic counter electronic components. These procedures are arranged to assist in locating a defective stage or circuit board that may not be functioning correctly during the performance check. Wherever possible, printed circuit boards and circuit assemblies are checked while operating in the instrument. This assures actual operating conditions and permits making performance checks with a minimum of external equipment.

39. Test Equipment Required

Recommended test equipment for performance chocks is listed in Table 11. Test equipment specification.

Cautions:

1. This equipment contains transistor circuits which may be damaged. If any equipment item does not have -in isolation transformer in its power supply circuit, connect one in the power input circuit. A suitable transformer is identified by FSN 5950-356-1779.

2. Never connect test equipment (other than oscilloscopes, Multimeters, and vtvm's) outputs directly to a transistor circuit; use a coupling capacitor.

3. Make test equipment connections with care so that shorts will not be caused by exposed test equipment connectors. When making contact to the circuit under test, tape or sleeve (spaghetti) test prods or clips to leave as little are; exposed is possible to make contact with the circuit under test.

4. The transistorized equipment must be turned off before removing a printed circuit board. The transient voltages, created by board removal, may exceed the punch-through rating of the transistors.

40. Test Equipment, Tools, and Materials

All test equipment required to perform the procedures given in this section are listed in Table 11. No special tools or materials ;re required other than the maintenance materials listed in paragraph 35.

41. Performance Checkout Procedure

The performance checkout is used to determine if the electronic counter or the display indicator is f4nctioning correctly. If the display indicator (or a mechanical printer) is connected to the electronic counter, all frequency indications will automatically be displayed on the display indicator or printed-out by the printer. Perform paragraph a if the electronic is rack mounted or paragraph b if the electronic counter is to be serviced at WI test bench area.

a. Rack Mounted Checkout. When the electronic counter is mounted in the rack, perform the performance checkout procedure given in Table 12. If the instrument should fail to provide the desired performance standard results, remove the instrument from service and perform applicable maintenance procedures. If the instrument meets all performance requirements, reconnect the signal input and control cables and return the instrument to service.

b. Test Bench Checkout. When the electronic counter performance checkout is performed at a test area do not perform step 1 of the performance checkout procedure given in Table 12. Connect the instrument to a convenient ac power source and perform steps 2 through 9 only.

Table 11. Test Equipment

Nomenclature	Federal Stock No.
Electronic Voltmeter, AN/USM-98	6625-753-2115
Oscilloscope, Tektronics 581, de to 85 Mc	
Oscilloscope, AN/USM-140	6625-066-2525
Signal Generator, AN/USM-44	6625-669-4031
Signal Generator, SG-511/U	6625-819-0472
Signal Generator, SG-340A/G	6625-539-9674
Signal Generator, SG-97/FRC	6625-351-5958

Table 12. Performance Checkout Procedure Chart

Step No.	Test Equipment Control Settings	Equipment Under Test Control Settings	Test Procedure	Performance Standard
1.	None	1-Mc EXT-INTERNAL switch set to INTERNAL position.	Disconnect the input cables connector J1, J2, and J3 on electronic counter rear panel, connect jumper coaxial cable between J1 and J5.	None
2.	None	Set POWER switch to ON position.	Connect jumper wire between J3-V and J3-K.	Readout indicates 9978.600 Mc.
3.	Adjust for 121.40 MHz; 1-volt rms	Same as steps 1 and 2.	a. Turn ON test equipment and allow a few minutes warm-up before proceeding.	None
			b. Apply R.F. oscillator output to J 1.	Readout indicates 0100.000Me, ±1 digit.
4.	Repeat step 3.	Same as steps 1 and 2.	Connect jumper wire between pins J3-V and J3- L.	Readout indicates 0100.000 Mc, ±1 digit.
5.	Repeat step 3 for 321.40 MHz. digit.	Same as steps 1 and 2.	Same as step 4.	Readout indicates 0300.000 Mc,±1
6.	Repeat step 3 for 360.40 MHz.	Same as steps 1 and 2.	Connect jumper wire between pins J3-V and J3-M; apply R. F. oscillator output to J2.	Readout indicates 0300.000 Mc,±1 digit.
7.	Repeat step 3 for 560.0 MHz.	Same as steps 1 and 2.	Repeat step 6.	Readout indicates 0500.000, ±1 digit.
8.	Repeat step 3 for 660.0 MHz.	Same as steps 1 and 2	Connect jumper wire between pins J3-V and J3-N.	Readout indicates 0600.000, ±1 digit.
9.	Repeat step 3 for 1.060 GHz	Same as steps 1 and 2.	Repeat step 8.	Readout indicates 1000.000 Mc, ±1 digit.
10.	Repeat step 9	Same as steps 1 and 2	Connect jumper wire between pins J3-V and J3-P.	Readout indicates 1060.000 Mc±1 digit.
11.	Repeat step 9 for 2.16 GHz.	Same as steps 1 and 2.	Repeat step 10.	2160.000 Mc, ±1 digit.

Section III. TROUBLESHOOTING

42. General

Troubleshooting of the electronic counter is based upon the performance checks. Maintenance troubleshooting procedures normally will be limited to the repair of parts and the replacement of printed circuit boards. This section includes troubleshooting information necessary to determine the nature of the repairs required. disassembly and assembly techniques necessary to effect the repair, and all testing procedures needed to assure serviceability of repaired items.

43. Troubleshooting

To troubleshoot the electronic counter, perform the step)s indicated in the troubleshooting chart Table 13. Perform all functions listed proceeding through the steps until an abnormal condition or result is observed. Schematic diagrams are included at the rear of this section. Part location illustrations are included in Chapter 8.

44. Troubleshooting Procedures

a. General. The first step in serviceing a defective electronic counter is to sectionalize the fault. Section alization means tracing the fault to a unit such as the power supply. The second step is to localize the fault. Localization means tracing the fault to a defective stage or circuit responsible for the abnormal condition. The third step is isolation. Isolation means the locating of the defective part or parts. Some defective parts, such as burned resistors and arcing shorted transformers can often be located by sight, smell, and hearing. Most defective parts, however, must be isolated by checking voltages and resistance.

b. Sectionalization. The electronic counter consists of a single unit with a separate remote display indicator unit. The first step in tracing trouble is to locate the unit or units at fault by the following methods:

(1) Visual Inspection. The purpose of visual inspection is to locate faults without testing or measuring circuits. All meter readings or other visual signs should be observed and an attempt made to sectionalize the fault to a particular unit.

(2) Operational tests. Operational tests frequently indicate the general location of trouble. In many instances, the tests will help in determining the exact nature of the fault. If the exact nature of the instrument malfunction is not known, perform the performance checkout procedures first.

c. Localization. Localization procedures should be performed after the trouble has been sectionalized (b above). The localization procedures applicable to this equipment are listed in (1) below, and should be used in localizing the trouble to a stage or module in the suspected unit.

(1) Troubleshooting chart. The troubleshooting chart Table 13, lists symptoms of common troubles and gives (or references) corrective measures. Such a chart obviously cannot include all trouble symptoms that may occur. The repairman should use this chart as a guide in analyzing symptoms that may not be listed.

d. Techniques. In performing the sectionalization, localization, and isolation procedures, one or more more of the techniques b-low may be applied. Apply these techniques only as indicated, and observe all 'cautions.

(1) Voltage measurements. This equipment is transistorized. When measuring voltages, use tape or sleeving (spaghetti) to insulate the entire test prod, except for the extreme tip. A momentary short can ruin a transistor.

(2) Waveforms Analysis.

(a.) Waveforms may be observed it various test points and connector pins in the circuits of the electronic counter. The normal waveforms obtained are shown in Chapter 4 on the applicable block diagrams and timing diagrams. By comparing the ideal observed waveforms with the normal waveforms, a malfunction sometimes will be isolated and located.

(b) A departure from the normal waveform indicates trouble between the point at which the waveform is observed to be normal and the point at which the waveform is observed to be abnormal. For example, if ; waveform is observed to be normal at the base of a stage, and abnormal at the collector or output of the same stage, it is an indication that trouble is in that stage.

(c) When trouble is indicated in a stage, check any other inputs to the printed circuit board to determine the first malfunction indication is not a result of a malfunction supplied by a second circuit. If all other inputs are normal, replace the printed circuit board before making any further tests. If replacing the printed circuit board does not correct the trouble, place the original printed circuit board back in the connector and take voltage and resistance measurements at the connector socket.

(d) Various printed circuit boards may be interchanged, however, only with like type boards. Printed circuit boards in the I Mc oscillator decade counters are interchangeable with the same part number printed circuit boards in the readout decade counter circuits. If the board is interchanged with a similar function but not the same part number (2.5 MHz DCU with a 250 KHz DCU) a drastic change in performance may occur,. This practice however is not recommended.

(e) When a waveform at a certain point is observed to be abnormal, the cause may be absence of a signal from another unit. The point to start checking wave forms is at the input connector. Caution: Before using any ohmmeter to test transistors or transistor circuits, check the open circuit, voltage across the ohmmeter test leads. Do not use the ohmmeter if the open-circuit voltage exceeds 1.5 volts. Also, since the RXI range normally connects the ohmmeter internal battery directly across the test leads, the comparatively high current (50 ma or more) may damage the transistor under test. As a general rule, the RXI range of any ohmmeter should not be used when testing low-powered transistors.

(3) Test points. Generally boards are equipped with test jacks to facilitate connection of test equipment to various units. The test points should be used whenever possible to avoid disassembly to the equipment. These test points are shown on the printed circuit board schematic diagrams (fig. 39 through 58) and on the parts location diagrams in Chapter 8.

(4) Intermittent troubles. In all the tests, the possibility of intermittent troubles should not be overlooked. If present, this type of trouble often may be made to appear by tapping or gently jarring the equipment. Make a visual inspection of all wiring and connections. Minute cracks in printed circuit boards can cause intermittent operation. A magnifying glass is often helpful in locating defects in printed boards. Continuity measurements of printed conductors may be made using the same technique ordinarily used on hidden conventional wiring.

45. Localizing Troubles

a. General. In the troubleshooting chart procedures are outlined for sectionalizing troubles to the power supply or to the electronic counter, and for localizing troubles to stage within the various sections of the electronic counter. Depending on the nature of the operational symptoms. one or more of the localizing procedures will be necessary. When trouble has been localized to a particular stage, use voltage and resistance measurements to isolate the trouble to a particular part.

b. Use of Chart. When an abnormal symptom has been observed in the equipment, look for a description of this symptom in the Symptom column and perform the corrective measure shown in the Checks and Corrective Measures Column.

c. Conditions for Tests. All checks outlined in the chart are to be conducted with the electronic counter connected to a power source as described in paragraph 46.

46. Test Setup

Bench tests of the electronic counter requires connections to a power source and to various test equipments. The power source must be connected to the electronic counter for all dynamic-serviceing procedures. The test equipment use will vary with input frequency covered. Remove the electronic counter top and bottom covers and made a test as outlined below:

Caution: Before making the connections observe the cautions in paragraph 49. Transistor damage may be avoided.

a. Electronic Counter.

(1) Disconnect the power and signal input cables on the rear of the instrument.

(2) Remove the instrument from the mounting rack and place on a convenient work bench in a repair area.

(3) Remove the cover as follows:

(a) Twist the locking screws mounted around the cover edge 1/4 turn counterclockwise to release the top cover.

(b) The bottom cover is removed in a similar manner, twisting each screw 1/4 turn counterclockwise to release the bottom cover.

(c) The top and bottom covers are installed by placing the individual cover over the mounting area and while gently pressing the cover in place, setting each screw with a 1/4 turn, in a clockwise direction to lock in position.

Note: The electronic counter and the display indicator are shielded for radio frequency interference (RFI). Make sure the covers are seated properly to prevent any radiation of spurious radio frequency interference signals.

(4) Make sure the POWER switch is in the OFF position. Connect the instrument to a convenient power source for use in bench tests.

(5) Perform the Troubleshooting Procedures in Table 13.

b. Display Indicator.

(1) Perform the Electronic Counter test set up procedures in paragraph 46.

(2) Using the 100 foot interconnection cable assembly, connect the display indicator to the electronic counter.

(3) Perform the Troubleshooting Procedures in Table 13.

Warning: Be careful when working on the 115-volt ac line and the +330-volt dc circuits. Serious injury or death may result from contact with these terminals.

Caution: During troubleshooting procedures it may be necessary to remove printed circuit boards from the electronic counter for testing. To avoid damage to these boards, refer to printed circuit board removal and replacement procedures given in paragraph 49.

Table 13. Troubleshooting Chart

Note: Conduct performance checks, Section 11 before using this chart, unless trouble has already been localized.

Step	Symptom	Probable Trouble	Checks and Corrective Measures
1	Decimal lamp does not light, blower fan does not operate.	a. Power cable loose.	Tighten power cable and check for 115 volts ac between pins I and 2 of line filter A49FL1.
		b. Line fuse defective.	Replace defective fuse A49F1.
		c. Decimal lamp defective.	Replace defective lamp A4811.
		d. POWER switch defective.	Replace defective switch A48S1.
		e. Blower fan defective.	Replace defective blower fan A49B1 (paragraph 49k).

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
2.	Readout indicator does not light.	a. Defective power transformer	Check power transformer A47TI. Replace if defective.
		b. Defective +330 volt de power supply circuit.	Troubleshoot and repair +330 volt power supply circuit.
3.	Readout glow-tubes do not light or are blinking erratically when POWER switch is set to ON.	a. No ac power is applied to the power supply.	a. Check for defective power input cable.
			b. Check fuse A49F1. If fuse continues to blow, check 115 volt ac input to I-MHz oscillator A47Y' and power transformer A47T 1.
			c. Troubleshoot power supply and replace defective components.
4.	Absence of +12 volts dc or out of tolerance.	a. Defective 4 12 volt de circuit.	Check for +12 t-0. 12 volts de at fuse A47F4; check 412 volts de circuit calibration (paragraph 50).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A 1.
5.	Absence of -12 volts de or out of tolerance.	a. Defective -12 volts de circuit.	Check for -12 t-0. 12 volts dc at fuse A47F3: -12 volts dc circuit calibration (paragraph 50).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A 1.
6.	Absence of +4.5 volts de or out of tolerance.	a. Defective +4.5 volts de circuit.	Check for +4.5 t0.045 volts de at fuse A47'F2. Check +4.5 volts de circuit calibration (paragraph 50).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A 1.
7.	Absence of -4.5 volts de or out of tolerance.	a. Defective -4.5 volts de circuit.	Check for -4.,5 ,0.045 volts dc at fuse A47FI. Check -4.5 volts dc circuit calibration (paragraph 50).
		b. Power supply regulator defective.	Check and replace defective power supply regulator A47A 1.
8.	Absence of 430 volts de or out of tolerance.	a. Defective +30 volts dc circuit.	Check for ,30 t0.3 volts de at pin 12 of A47A1.
		b. Defective power supply regulator.	Check and replace defective power supply regulator A47AI.
9.	Any one readout glow-tube defective; decimal lamp lights.	The associated memory readout circuit defective.	Replace memory readout A10, A12, A14, A16, Al18, or A20 (paragraph 49 c). Check the associated counter unit.
		Defective glow-tube.	Replace glow-tube.

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
10.	Readout indicator lights but does not index.	Defective counter unit	Check and replace defective counter unit A 11 A13, A15, A17, A19, or A21.
11.	Readout indication frequency measurement inaccurate.	1-MHz oscillator defective or out of tolerance.	Check for 1.0 MHz ± 2(0Hz at J3 wan electronic counter. If out of tolerance, perform calibration procedure paragraph 50.
12.	Absence of l-Mhz oscillator output at J3 ro out of tolerance.	a. Defective 1-Mhz oscillator	Check 1-MHz oscillator calibration (paragraph 60).
		b. Defective +12 volts de circuit.	Check and repair + 12 volt dc circuit.
13.	Readout indication frequency measurements repeated consistency error indication	Insufficient input signal.	Check and adjust input signal for I volt rms maximum.
14.	Electronic counter functions on channel I but repeated consistency error indication on other channels.	a. Repeat step 13.	Repeat step 13.
		b. Coaxial switch defective.	Connect multimeter, (adjusted for ,12 volt de) between pin A50PA45-2 and chassis ground. Connect jumper wire between J3-V and J3-K and observe multimeter indication changes. If multimeter indication remains the same, replace coaxial switch A48A1S1 (paragraph 49 h).
		c. Relay A48K1 defective.	Connect multimeter (adjusted for +12 volts de) between A50P45-18 and chassis ground. Connect jumper wire between J3-V and J3-K. Observe that multimeter indicates +11 ± 2 volts dc and relay A48K1 is actuated. If multimeter indication is much below +11 volts, replace remote operation buffer A45 (paragraph 49)b. If relay A48KI fails to actuate, replace relay (paragraph 49 i).
		d. Relay A48K2 defective.	Connect multimeter (adjusted for 4 12 volts de) between pin A50P45-5 and chassis ground. Connect jumper wire between J3-V and J3-N and observe that multimeter indicates 11 ±2 volts de and relay A48K2 is actuated. If multimeter indication is much below . 12 volts, replace remote operation buffer A45 (paragraph 49 b). If relay A48K2 fails to actuate, replace relay (paragraph 49 1).
		e. C.U. circuit defective.	Check C. U. circuit output at pin A5-2 with an oscilloscope. If signal is steadv (not changing or erratic), circuit is functioning correctly.

Note: Connect the oscilloscope external sync input to pin A50P36-12 For all waveform measurements. All waveform parameters appear on applicable block diagrams in Chapter 4.

Table 13.. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
14, (Cons,)		f. C. U. circuit output erratic.	Disconnect N-Timing gate input from ratio and control circuit. If C. U. circuit starts to function correctly, that is. Begins divide by ten in a non-erratic fashion. replace ratio and control circuit A30 (paragraph 49 b). If readout indication still erratic or malfunctioning, replace C. U. circuit A5-A24 (paragraph 49 b).
15.	Erratic measurements. Repeated consistency observe error indication on channels II through V.	a. Input sampler circuits.	Connect an oscilloscope to test point 3 on the ratio gate circuit (A30) and waveform. If waveform is present and constant, I.C., S.C., F.S., I.S..and ratio gate circuits are functioning correctly.
		b. I. C. circuit defective.	Connect an oscilloscope to test point located on rear end of I. C. circuit and observe waveform. If waveform is present and constant, I. C. circuit is functioning correctly. If waveform is absent or shifting, replace I. C. circuit A3 (paragraph 49 b).
	Note: If troubleshooting checks determine the I. C. circuit or the 1. S. circuit printed circuit boards are defective and require replacing, it is recommended (although not mandatory) that replacement be done as a set. The I. C, and 1. S. circuit boards are adjusted at the factory as a set for best results. A serial number is then affixed to each pair of boards for identification of the matched pairs.		
		c. S. C. circuit defective. I. C. circuit functioning correctly.	Connect an oscilloscope to S. C. circuit rear connector and observe output waveform, If waveform is present and constant with a frequency between 9 and 10 MHz, S. C. circuit is functioning correctly. If wave form is absent or shifting, replace S. C. circuit A4 (paragraph 49 b.) (This wave form may shift and still be functioning correctly.)
		d. F.S. circuit defective.	Connect an oscilloscope to pin A50P1-17 and observe waveform. Frequency is 1.5 +0. 1KHz. Connect the oscilloscope to F.S. circuit output cable and observe waveform, If waveforms are present for each check, the circuit is functioning correctly. (This waveform may shift and still be functioning correctly.) If wave forms are absent or out-of-tolerance, replace F.S. circuit A1-A24 (para graph 49 b).
		e, I. S. circuit (or power divider defective.)	Connect an oscilloscope to pin A50P32-G and observe the I. S. circuit output wave form. If waveform is present and continuous, the I. S. circuit is functioning correctly. IL waveform is weak or absent. perform a continuity check of power divid er input and output cable assemblies and cable connector s. If waveform remains

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
15. (Cont.)			weak or absent after the continuity check, replace I. S. circuit A32 (paragraph 49b). If after performing the above check satisfactory results are not obtained, replace power divider A48A1ZI.
16.	Input sampler circuits functioning correctly at ratio gate test point 3 although measurement errors continue to occur.	a. Ratio gate or A logic circuits defective.	a. Connect the oscilloscope external sync to pin A50P30-13 and observe the ratio gate pulse input to the ratio gate circuit. Observe that the ratio gate pulse is a division-by-2 or a division-by-8 of the f2 (1.5 KHz) frequency.
	Note: All checks of the ratio gate circuit, A logic circuit, B logic circuit, and the display timer in the reset circuit, should be synchronized to the ratio gate pulse at pin A50P30-13.		
			b. If the ratio gate pulse is present at pin A50P30-13. check the ratio gate circuit output at pin A50P30-17. The ratio gate output will present groups of pulses with a repetition rate that will be the same as observed at pin A50P30-13. If input is absent, check and replace A logic circuit A25 (paragraph 49 b). If waveform at A50P30-17 is absent, replace the ratio gate circuit A30)paragraph 19 b).
17.	Consistency error indications fail to occur when error exists. and d.	a. B logic circuit defective.	a. Connect an oscilloscope to pin A50P27- 6 and observe waveform. If waveform is absent, repeat step) 15
			b. If waveform is present, (groups of pulses as in step) 16 b), check B logic circuit ouputs at pins at A50P26-17 and A50P27-11.
			c. If single burst-of-N pulses are present. circuit is functioning correctly. If waveform pulses are absent. replace B logic circuit A27 (paragraph 49 b).
			d. If waveform is present at A50P27-11 (the single burst-of-N pulses) circuit is functioning correctly. If waveform is absent, replace B logic circuit A27 (paragraph 49 b).
		b. Parity logic circuit defective. (1) Absence of single burst-of-N pulse.	Connect an oscilloscope to pin A50P26-16 and observe waveform. If1 waveform is present and varies only when input frequency to display indicator is varied, parity logic circuit is functioning correctly. If waveform varies, replace parity logic circuit A26 (paragraph 49 b). If waveform is absent, check waveform presents at pin A50P26-13. If waveform is present

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17 (Cont.)			at A50P26-13 replace parity logic circuit A26 (paragraph 49 b). If waveform is absent, check for 1-MHz pulses at pin A50P26-14. If waveform is present, replace parity logic circuit A26 (paragraph 49 b); if waveform is absent, repeat step 17 a.
		(2) Absence of error reset pulse.	Connect the oscilloscope to pin A50(1'26- and -observe waveform. If waveform is present only when the input frequency to, the electronic counter is varied, the parity logic circuit is functioning correctly. If waveform is present regardless of the adjustment to the display indi cator inputfrequency, replace the parity logic circuit A26 (paragraph 49 b).
		(3) Absence of A reset pulse.	Connect an oscilloscope to pin A501'26-6 and observe waveform. If waveform is present, A reset pulse circuit is functioning correctly. If waveform is absent. replace parity logic circuit A26 (paragraph 49 b.
		(4) Absence of greater-than four pulse.	Connect an oscilloscope to pin A50(26(-1 I1 and observe waveform. If waveform is present, parity logic, ratio and control and 2.5 MHz DCU (A38) are functioning correctly. If waveform is absent, check for waveform at pin A50P37-11. If waveform is present, replace 2.5 MHz DCU (A38). If waveform is absent, repeat step 17 b (1). If waveform is present in step 17 b (1), replace ratio, and control circuit A37 (paragraph 49 b).
		c. 1-MHz oscillator defective.	a. Connect an oscilloscope to pin A50P37-17 and observe waveform. If waveform is present, 1-MHz oscillator is functioning correctly. If waveform is absent, repair or replace I-MHz oscillator A47Y9.
			b. Connect an oscilloscope to pin A50P37-14 and observe wave(form. If waveform is present, 1-MHz wave shaping circuit is functioning correctlv. If waveform is absent, replace ratio and control circuit A37 (paragraph graph 49 b).
		d. 1-MHz oscillator time.-base generator circuit defective.	a. Connect in Oscilloscope to pin A50P37-15 and observe 1Khz ,pulses. If pulses are present, 2.5 MHz DCUs (A40, A41, and A42) are functioning Correctly. If waveform is absent, -proceed to step b.

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17. (Cont.)			b. Connect an oscilloscope to pin A50P42-7 and observe 10-KHz pulses. If waveform is present, replace 2.5 MHz DCU A42 paragraph 49 b).
		Note: The term DCU is used to denote ;a decade counting unit.	
			c. Connect an oscilloscope to pin A50P41-7 and observe 100-KHz pulses. If waveform is present, replace 2.5 MHz DCU A41 (paragraph 49 b). If waveform is absent, proceed to step d.
			d. Connect an oscilloscope to pin A5OP40-7 and observe 1-MHz pulses. If pulses are present, replace 2.5 MHz DCU A40 (paragraph 49 b). If waveform is al)sent, repeat I-MHz oscillator check.
			e. Connect an oscilloscope to pin A50P44-6 and observe 10Hz pulses. If waveform is present 2.5 DCUs A43 and A44 are functioning correctly. If waveform is al)sent, proceed to step f.
			f. Connect an oscilloscop,2 to pin A50P44-7 and observe 100 Hz pulses. If waveform is present, replace 2.5 MHz DCU A44 (paragraph 49 1). If pulses are absent, proceed to step g.
			g. Connect an oscilloscope to pin A50P43-7 and observe 1-KHz pulses mixed with 1-MHz pulses. If wave-form is absent, and steps a and d checks are satisfactory, proceed to step h.
			h. Connect an oscilloscope to pin A50P37-12 and observe the reset pulse. If reset pulse is absent, perform a checkout of the reset circuit. If the reset pulse is present, connect the oscilloscope to A50P37-10 and observe waveform. If both waveforms are present bit step g fails, replace the ratio ,:n(i control circuit A:37 (paragraph .!t b). If waveform atA50P1':7-10 is absent perform ratio DCUs A38 an(t A39 checkout procedure.
		e. Ratio DCUs de-fective.	a. Connect an oscilloscope' to) pin A50P39-7 and observe waveform. If waveform is present, but is not present at A50P37-10 in step h, replace 250 KHz DCU A:39 (paragraph 49 b). If waveform is absent, proceed to step b.

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17			b. Connect oscilloscope :to pin (Cont.) A50P38-7 and observe waveform. If waveform is present, replace 2.5 MHz DCU A38 paragraph 49 b). If waveform is absent, replace the ratio and control circuit A37 paragraph 49 b.
			c. Repeat the greater-than-lour pulse-check for the parity logic circuit.
		f. Ratio and control circuit start-stop multivibrator defective.	a. Connect an oscilloscope at N-Timing gate pulse test point 1 and observe waveform. Vary the input frequency applied to the display indicator and observe that waveform pulse-width will change. If the waveform is absent, check the pulse input at pin A50P37-2 and A50P37-12.
			b. Connect an oscilloscope to pin A50P37-2 and observe waveform. If waveform is present and time. interval between pulses changes as the display indicator input frequency is varied, DCUs A40, A41, A42, A43 and A44 are functioning correctly and providing nine-carry pulse outputs; proceed to step d. If waveform is absent, proceed to step c.
			c. If waveform is absent in step b, but time base, generator circuit check is satisfactory, successively remove DCUs A41 through A44 (in the reverse order) until the. nine-carry pulse occurs. If after removing ;l DCU the nine-carry pulse returns, replace the defective DCU With a new one paragraph 49 b). Adjust the oscilloscope sweep rate to display two nine carry pulse. Observe as a DCU is replaced in the time -base generator circuit. The time interval between pulses will increase by ten times. (As DCUs are removed the time interval between pulses will decrease by nine-tenths.) Replace any defective DCU (paragraph 49 b).
			d. Connect an oscilloscope to pin A50P37 - 12 and observe reset pulse. If the reset pulse and the nine-carry pulse are absent, in the N-Timing pulse is absent in step a, replace the ratio and control circuit A37 (paragraph 49 b).

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17. (Cont.)		g. Reset circuit defective.	a. Connect an oscilloscope to pin A50P36-14 and observe the positive reset pulse. Connect the oscilloscope to pin A50P36-12 and observe the negative reset pulse. If either pulse is absent, replace the reset circuit A36 (paragraph 49 b).
			b. Connect the oscilloscope pin A50P36-11 and observe the read pulse waveform. If the read pulse is present, the reset circuit display timer is functioning correctly. If the read pulse is absent, connect the oscilloscope to pin A50P36-4 and observe the stop flip-flo,) pulse is absent, replace the ratio and control circuit A37 (paragraphs 49 b). If the pulse is present, perform step c.
			c. Connect an oscilloscope to pin A50P36-16 and obserfe the f2 sync waveform. If the pulse is present and the pulse requirements of step) are present, replace the reset circuit A36 (paragraph 49 b.) If the f2 sync pulse is absent, perform the F.S. circuit check step 15.
		h. N-Ratio function defective.	Connect an oscilloscope to pin A50P29-2. Disconnect the RF input to the display indicator. Adjust the oscilloscope controls for a slow-sweep-scan and observe the display (N-Ratio pulse) varies as :t sawtooth voltage. If the waveform is present, the N-Ratio function circuits are functioning correctly. If the waveform is absent, perform the A.D. circuit checkout procedure.
		(1) A.D. circuit defective.	a. Connect an oscilloscope to pin A50P29-16. Vary the RF input frequency to the display indicator and observe that the oscilloscope display will present a series of pulses. If the pulses are present while the RF input is being varied, and are absent after the RF adjusting is stopped, the A.D. circuit is functioning correctly. If the pulses are present although the RF input is not being varied, proceed to step b.
			b. Connect an oscilloscope to pin A50P29-17. Disconnect the RF input to the electronic counter. (Make sure the oscilloscope sweep is synchronized to the reset pulse). Observe that the oscilloscope displays

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17. (Cont.)			the error reset pulse waveform. if the error reset pulse is absent, i-e-peat the parity logic circuit A2f6 checkout procedure. If the waveforms are present, proceed to stl1) c.
			c. Connect the oscilloscope input to A50P36-14 and observe the display pulse waveform. If waveform is absent, repeat ratio and control circuit A37 start-stop multivibrator checkout procedure. If waveform is present, observe the error reset pulses occurrence interval is coinci-dent (at random intervals) with the display pulse. If waveforms are coincident, and no output pulse is generated in step a, replace the A.D. circuit A29 paragraph 49 b).
		(2) Ramp generator circuit defective.	Connect an oscilloscope to pin A50P29-2 and disconnect the RF input to the electronic counter. Adjust the oscillo scope for a slow-sweep-scan and observe that the oscilloscope display (N-Ratio pulse) varies as a sawtooth voltage. If the voltage fails to vary as a sawtooth (or has steps in the waveform), succes-sively connect the oscilloscope to pins 10, 11, 13, 14, 15, 16, and 17 of A50P33 and observe that a binary division waveforms occur. If all waveforms are I)present, replace the ramp generator circuit A3:; (paragraph 49 b). If a step in the sawtooth waveform occurs or a binary division does not occur at pins 10, 11, 13, or 14 of A5OP33, perform the divide-by- 16 A34 checkout procedure. If a binary does not occur at pins 15, 16 or 17, or A5OP33, perform the divide-by-8 circuit (A35) checkout procedure.
		(3) Divide-by-1(i circuit defective.	Connect an oscilloscope to p1in A50P34-6 and observe waveform. If pulses are present, while no binary division occurs at Pins 10, 11, 13 and 14 of A50P33, replace the divide-by 16 circuit A34 (paragraph 49 b). if all the binary divisions occur, perform the divide-by-8 circuit (A35) checkout procedure.
		(4) Divide-by-8 circuit defect.	Connect an oscilloscope to pin A50OP:3.-(; and observe waveform. If waveform is absent, replace the divide-by 16 circuit paragraph 49 b). If the waveform is present, successively connect the oscilloscope to pins 15, 16, 17 of A50P33 and observe that a binary division waveform occurs. If all the waveforms are present, replace the ramp generator circuit A33 paragraph 49 b).

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
17. (Cont.)			If a binary division does not occur at pins 15, 16, or 17, replace the divide-by-8 circuit A35 (paragraph 49 b).
18.	Preset offset inoperative or in error.	a. Remote operation buffer defective.	Perform checkout of coaxial switch and relays A48K1 and A48K2 in step 14
		b. -21.40 MHz preset generator circuit defective.	a. Connect a jumper wire between pins V and K of connector J3. Connect an oscilloscope input to pin A50P22-C and observe the -Reset pulse waveform. Adjust the waveform off-time to occur one third distance across the oscilloscope screen. If -Reset pulse is absent, repeat reset circuit A36 checkout procedure in step 17. If waveform is present, proceed to step b. b. Connect a multimeter to A50P22-16 and measure 11±2 volts dc. If voltage is present, proceed to step c. If voltage is absent, repeat remote operation buffer circuit checkout procedure. c. Connect the oscilloscope input to pin A50P22-18 and observe the Preset pulse waveform. Observe the Preset pulse will occur immediately after the -Reset pulse occurs. If the Preset pulse is present, proceed to step d. If Preset pulse is absent, replace -21.40 MHz preset generator (paragraph 49 b) and repeat step a. d. If the Preset pulse is present in step c successively connect the oscilloscope second input to pins 6, 8, 10, 11, 15, H, K, L, P, and R of AP50P22. Observe the Preset pulse. If the Preset pulse is present at all the pins, the -21.40 MHz preset generator is functioning correctly. If any one preset pulse is absent, replace the -21.40MHz preset generator circuit (paragraph 49 b).
		c. -60.0 MHz preset generator circuit defective.	a. Connect a jumper wire between pins V and M of connector J3. Connect an oscilloscope input to pin A50P23-C and observe the -Reset pulse waveform. Adjust the waveform off-time to occur one-third distance across the oscilloscope screen. If -Reset pulse is absent, repeat reset circuit A36 checkout procedure in step 17. If waveform is present, proceed to step b.

Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
18. (Cont.)			b. Connect a multimeter to A50P23-15 and measure 11 ±2 volts de. If the voltage is present, proceed to step c. If voltage is absent. replace remote operation buffer circuit checkout procedure. c. Connect the oscilloscope input to pin A.,OP23-18 and observe the Preset pulse waveform. Observe the preset pulse will occur immediately after the -Reset pulse occurs. If the Preset pulse is present, proceed to step d. If the Preset pulse is absent, replace -60.0 MHz preset generator (paragraph 49 b1)) and repeat step a. d. If the Preset pulse is present in step) a, successively connect the oscilloscope second input to pins 6, 8, K, and L of A50P23 and observe the Preset pulse. If the Preset pulse is present at all pins, the -(i6 MHz I)reset generator is functioning correctly. If any one preset pulse is absent, replace the -60.0 MHz preset generator circuit (paragraph 49).
19.	Readout display is in error or fails to index correctly.	a. Read pulse is defective.	Connect an oscilloscope to pin A50P10-1S. Vary the RF oscillator input and observe the read pulse waveform on the oscilloscope. If the read pulse is present, the display circuit read pulse circuit is functioning correctly. If the read pulse is absent, perform a checkout of the reset circuit A36.
	Note: The counter checks (A11, A13, A15, A17, A19 and A21) in the totalizing chain and the associated memory readout circuits (A10, A12 A14, A16, A18, and A20) checkout procedures are similar. Each counter provides a division-by-10 of the frequency applied to its input. Preliminary circuit checks may be made by substituting the same part number board in a socket for a suspected board.		
		b. Any one or more memory readout circuits are defective.	a. Turn OFF the electronic counter POWER and remove p)reset circuit boards A22 and A23. Connect an RF oscillator, adjusted for 222. 2220 MHz,1 volt rms input signal, to connector J1. Connect : jumper wire between pins J3-V and J3-K. Turn ON the POWER and observe that the electronic counter readout indicates 222.2220 Mc. If the readout indicates as specified, channel 1 is functioning correctly. If the readout display indication is in error although the readout appears to be functioning correctly when the input

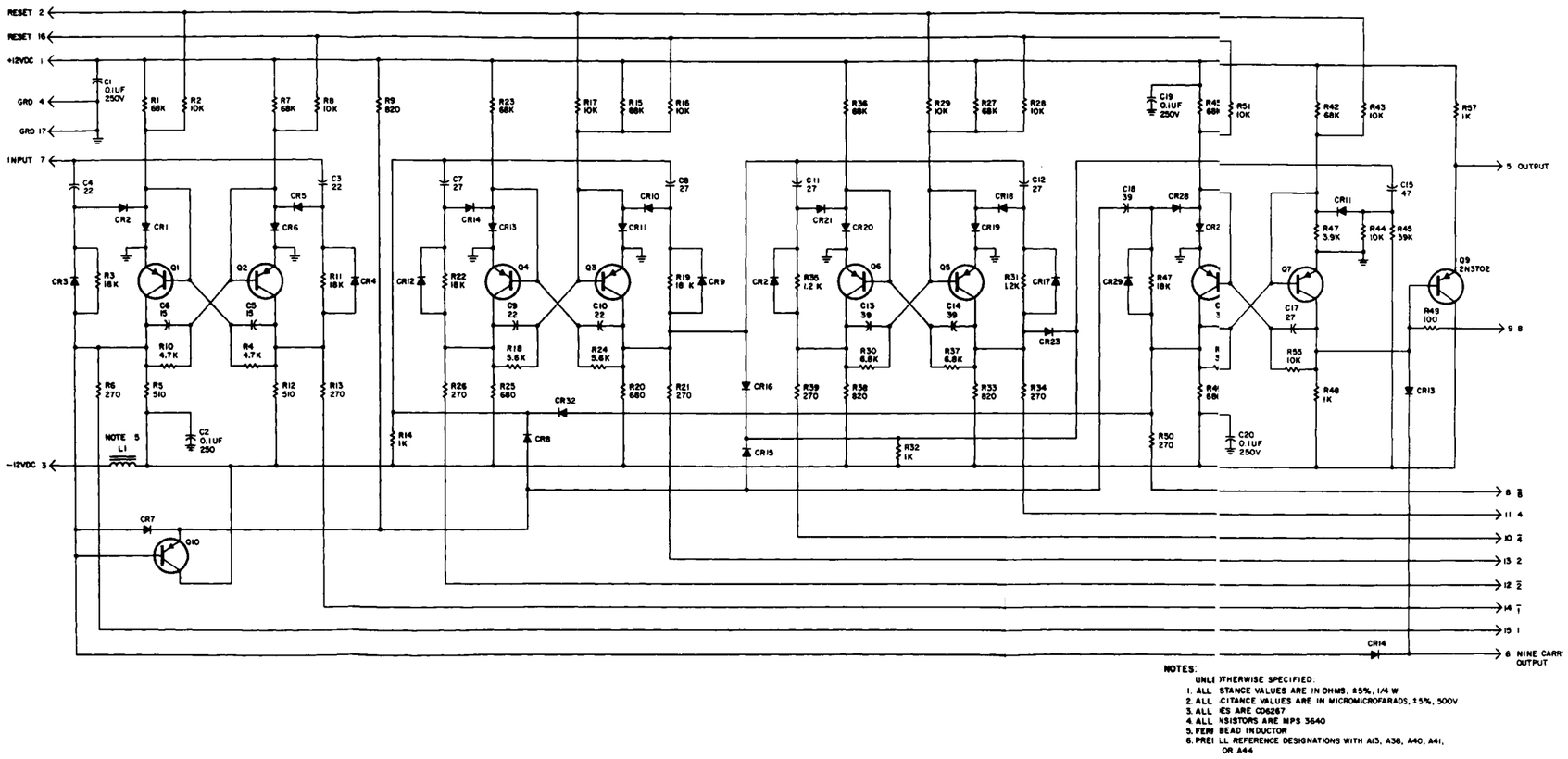
Table 13. Troubleshooting Chart (Cont.)

Step	Symptom	Probable Trouble	Checks and Corrective Measures
19. (Cont.)			RF oscillator frequency is varied, repeat the 1-Milz oscillator check, step 11. If the readout display indication is correct on channel 1, perform channel II through V check-out steps 14 through 18. If the individual memory readout circuit is malfunctioning regardless of the above checks, proceed to step b.
			b. Adjusting the RF oscillator for 222.2220 MHz output. Successively connect the oscilloscope input to pins 9, 11, 13, and 15, A50P20 and observe the BCD output from the counter as shown on the 250-Kllz decade counting unit timing function diagram in Chapter 4. If waveform appear as shown in the figure, the counter is functioning correctly. Replace the memory readout circuit A20 (paragraph 49 c. Memory readout A10, A12, A14, A16, and A18 are checked out in a similar manner at their respective sockets, If any timing function is incorrect, perform the decade counter checkout. Proceed to step c to checkout memory readout circuit A8 and the matrix circuit A7.
			c. Perform the same checkout of memory readout A8 as performed in step b at A5,OP8. (Refer to matrix circuit A7 timing functions figure for BCD input waveforms.) If waveforms appear as shown in the figure, C.U. circuit and the matrix circuit are functioning correctly. Replace memory readout A8 (paragraph 49 c). If any timing function is incorrect, perform the matrix circuit checkout procedure.
		c. Matrix circuit defective.	Perform the C.U. circuit checkout procedures in step 14. If the C.U. circuit is functioning correctly, successively connect an oscilloscope input to pins 16, 6, 7, 17, and 2, and observe the quinary output from the C.U. circuit. (Refer to matrix circuit A7 timing functions figure for quinary input waveforms.) If waveforms appear as shown in the figure, the C.U. circuit is functioning correctly. Replace matrix circuit A7 (paragraph 49 b). If the waveforms are abnormal or absent, replace the C. U. circuit (paragraph 49 b).

Table 13. Troubleshooting Chart (Cont.)

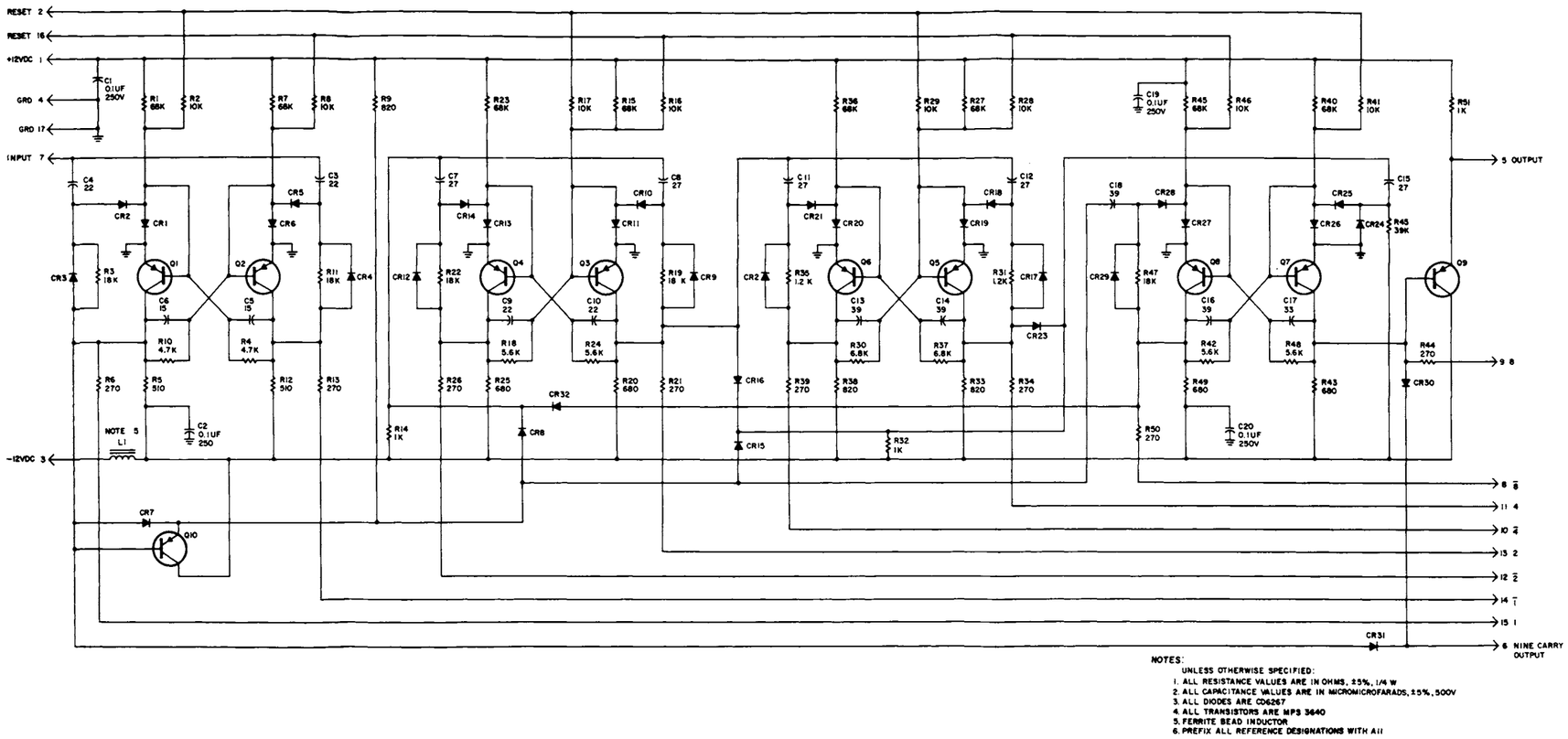
Step	Symptom	Probable Trouble	Checks and Corrective Measures
19. (Cont.)		d. Totalizer decade counter defective.	a. Connect an oscilloscope to pin A50P21-7. Adjust the oscilloscope controls for 10 pulses presentation. Connect the second input to the oscilloscope to pin A50P21-5 and observe a single output pulse waveform. (A division-by-10 occurs as shown on the associated timing function diagram in Chapter 4.) If a division-by-10 occurs correctly, proceed to step b. If the division-by-10 fails to occur, replace the decade counting unit (paragraph 49 b). b. Successively connect an oscilloscope to pins 9, 11, 13, and 15 of A50P21 and observe the BCD output from the counter as shown on MHz decade counting unit timing function diagram in Chapter 4. If waveforms appear as shown in the figure, the counter is functioning correctly. If the divide-by-10 pulse is produced in step a, but the waveforms in step b are absent or incorrect, replace the decade counting unit paragraph 49 b .

Note: The three types of decade counting units are checked out in a similar manner as detailed above. When the NOT function output is used, pins 8, 10, 12, and 14 are used. If the ninecarry function is used, pin 6 provides the output pulse.



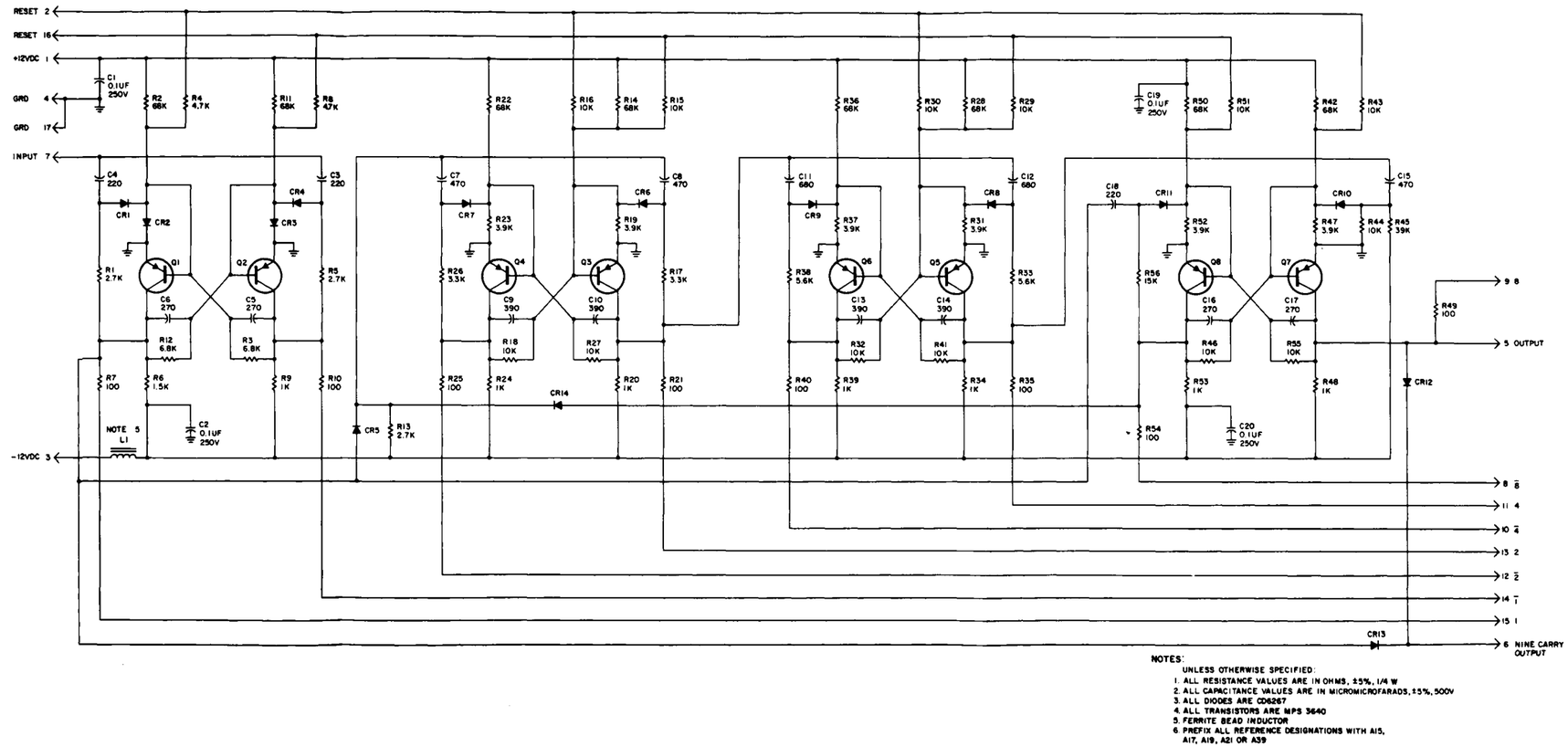
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 500V
3. ALL DIODES ARE CD4267
4. ALL TRANSISTORS ARE MPS 3640
5. FERRITE BEAD INDUCTOR
6. PREFIX ALL REFERENCE DESIGNATIONS WITH A13, A38, A40, A41, OR A44

Figure 39. 25-MHz Decade Counting Unit, Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 500V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE MPS 3640
5. FERRITE BEAD INDUCTOR
6. PREFIX ALL REFERENCE DESIGNATIONS WITH A11

Figure 40. 2.5-MHz Decade Counting Unit, Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 500V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE MPS 3640
5. FERRITE BEAD INDUCTOR
6. PREFIX ALL REFERENCE DESIGNATIONS WITH A15, A17, A19, A21 OR A39

Figure 41. 250- KHz Decade Counting Unit, Schematic Diagram

MAINTENANCE

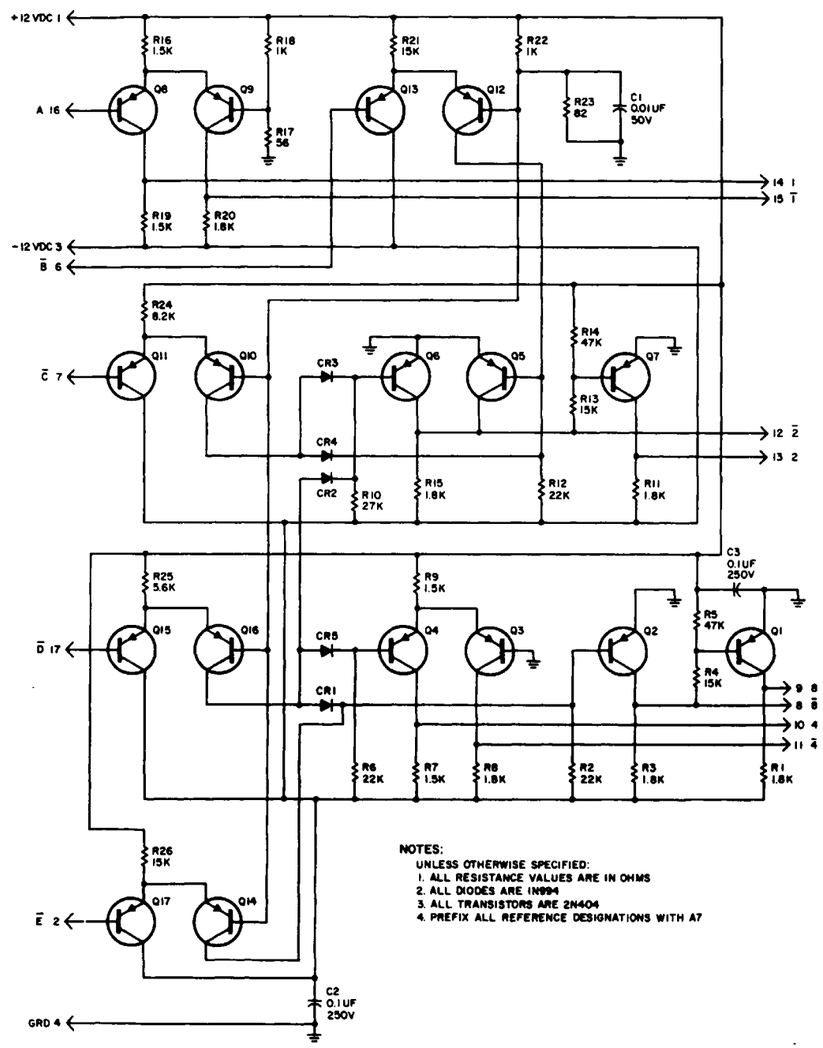
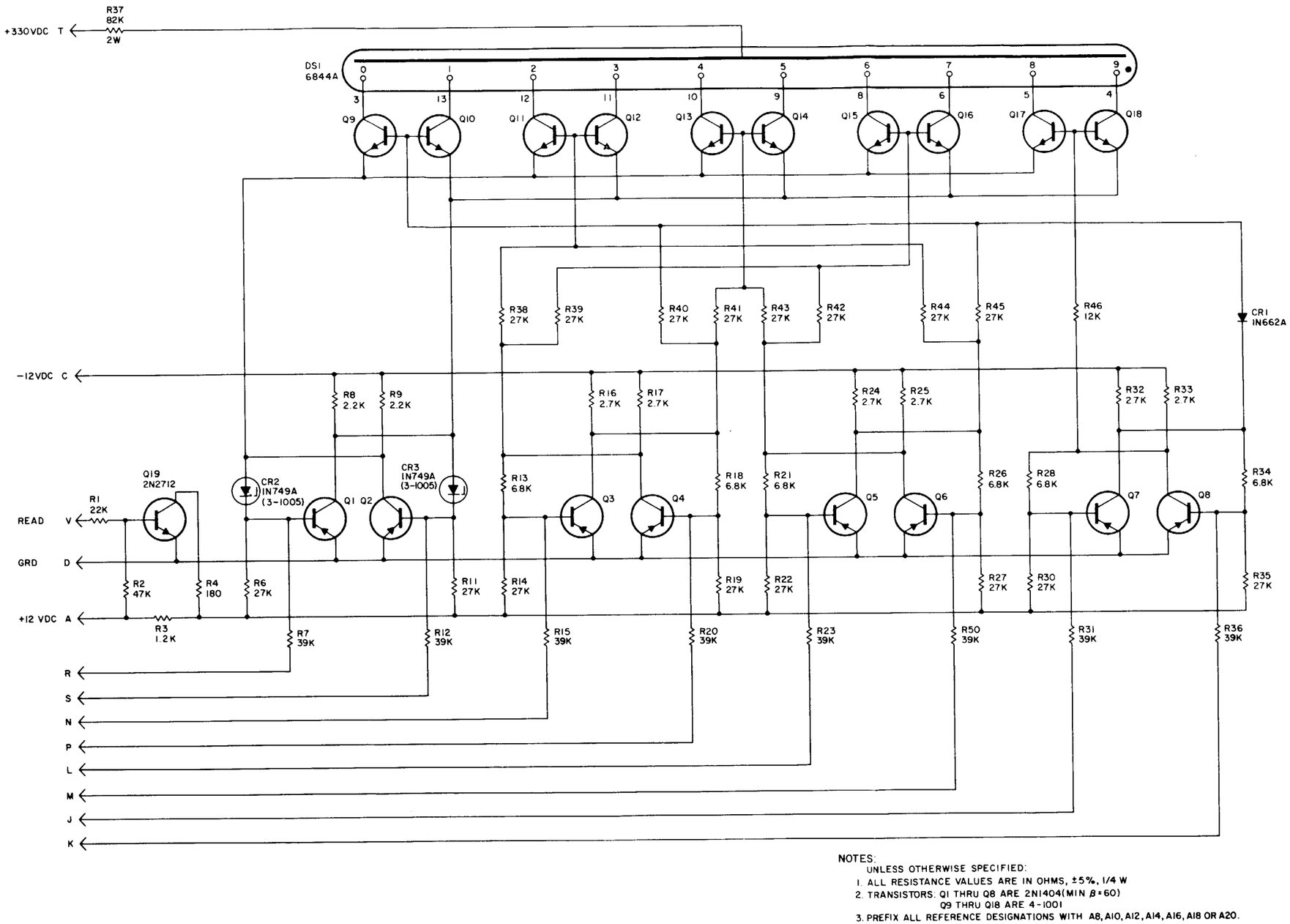
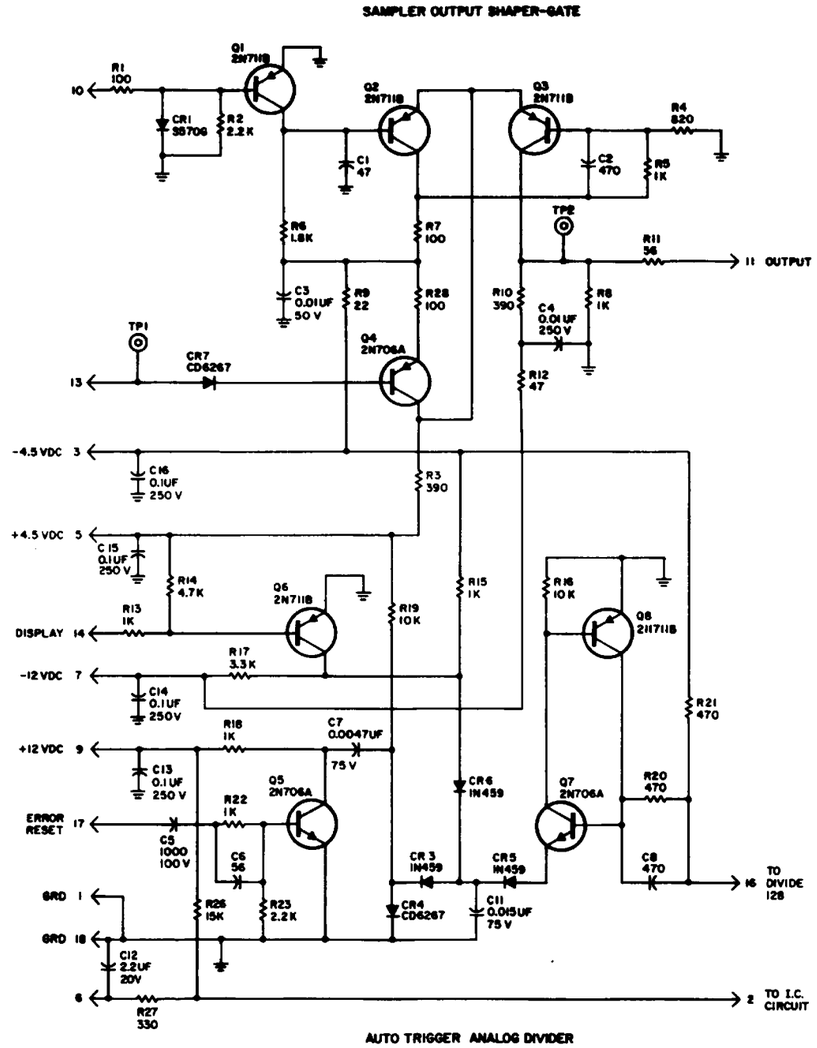


Figure 42. Matrix Circuit, Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. TRANSISTORS: Q1 THRU Q8 ARE 2N1404(MIN β=60)
Q9 THRU Q18 ARE 4-1001
3. PREFIX ALL REFERENCE DESIGNATIONS WITH A8, A10, A12, A14, A16, A18 OR A20.

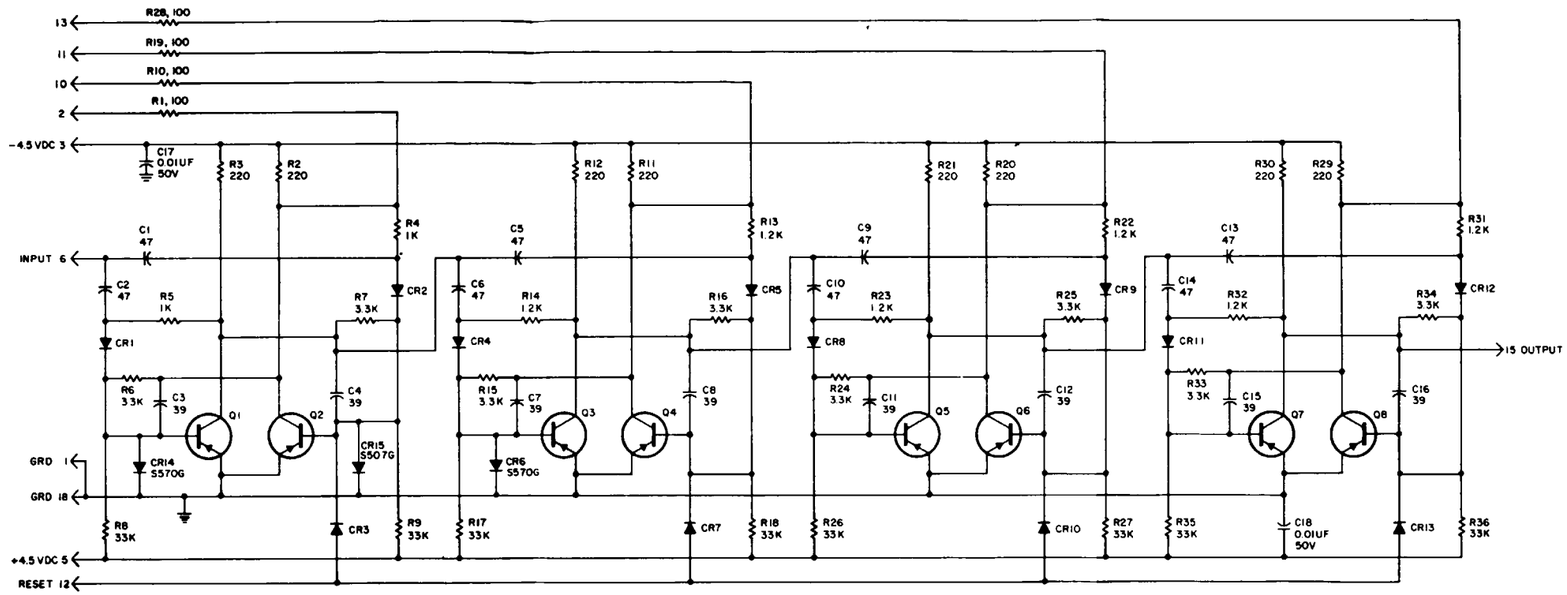
Figure 43. Memory Readout, Schematic Diagram



AUTO TRIGGER ANALOG DIVIDER

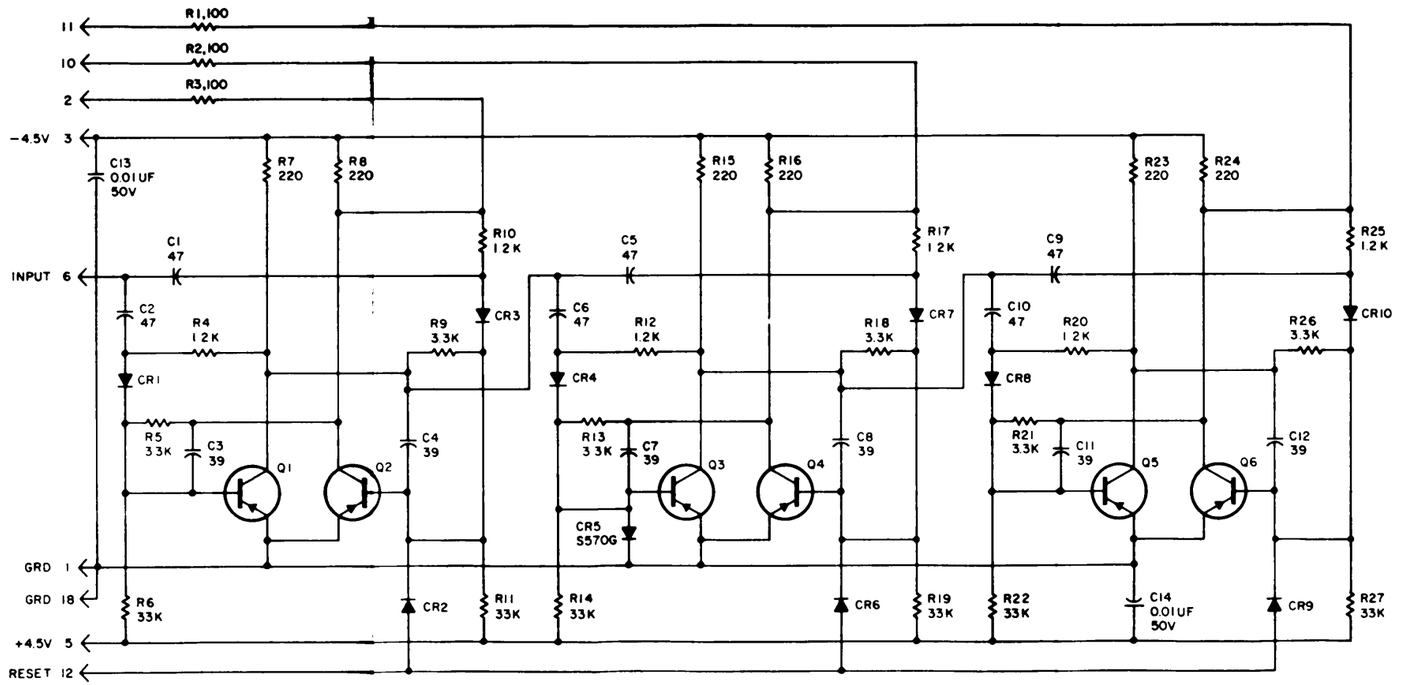
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS.
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, 500 V, ±5%.
3. PREFIX ALL REFERENCE DESIGNATIONS WITH A29.

Figure 44. A. D. Circuit Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 500V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE 2N711B (4-1003)
5. PREFEX ALL REFERENCE DESIGNATIONS WITH A34

Figure 45. Divide-by-16, Schematic Diagram

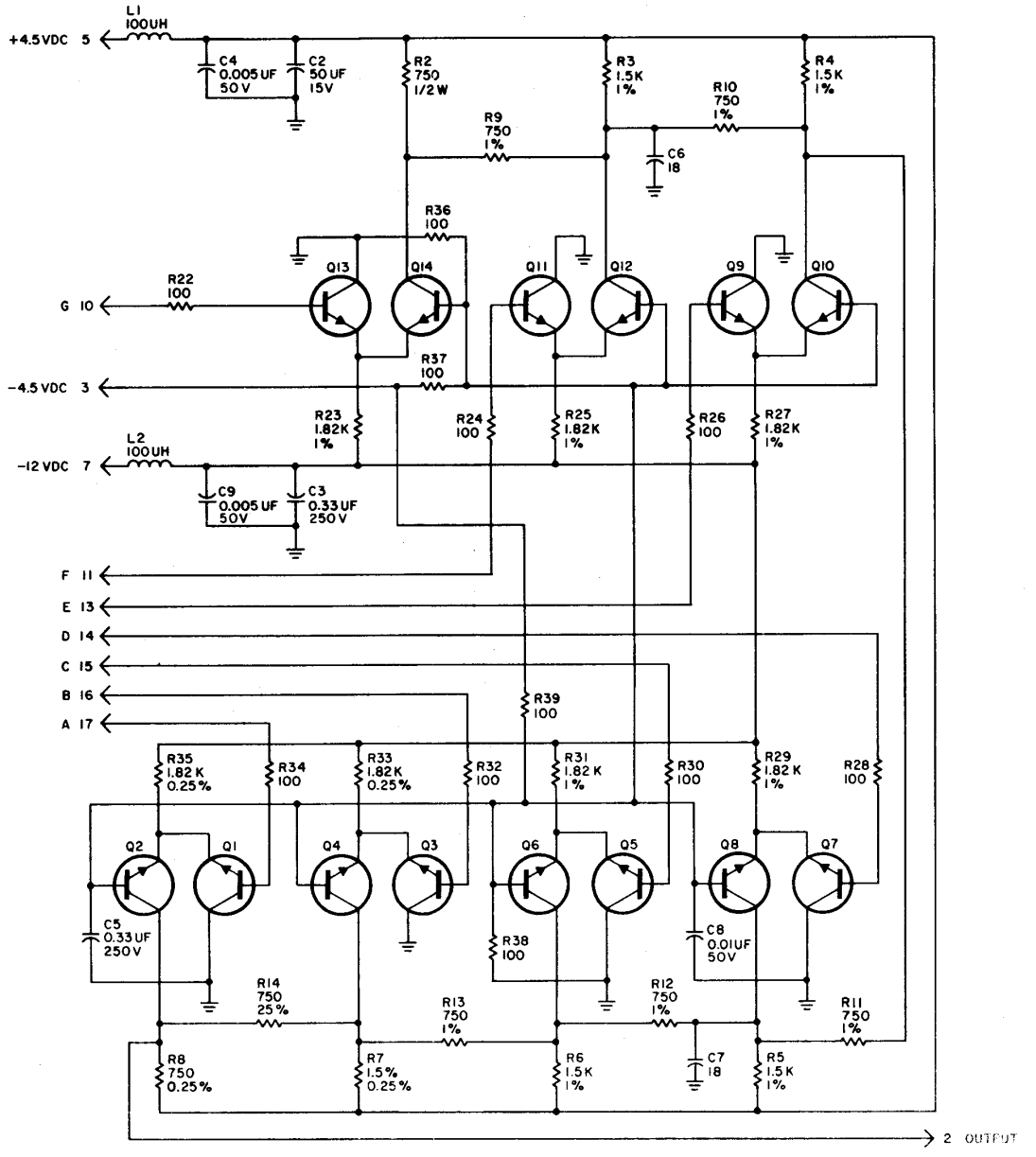


NOTES:

UNLESS OTHERWISE SPECIFIED:

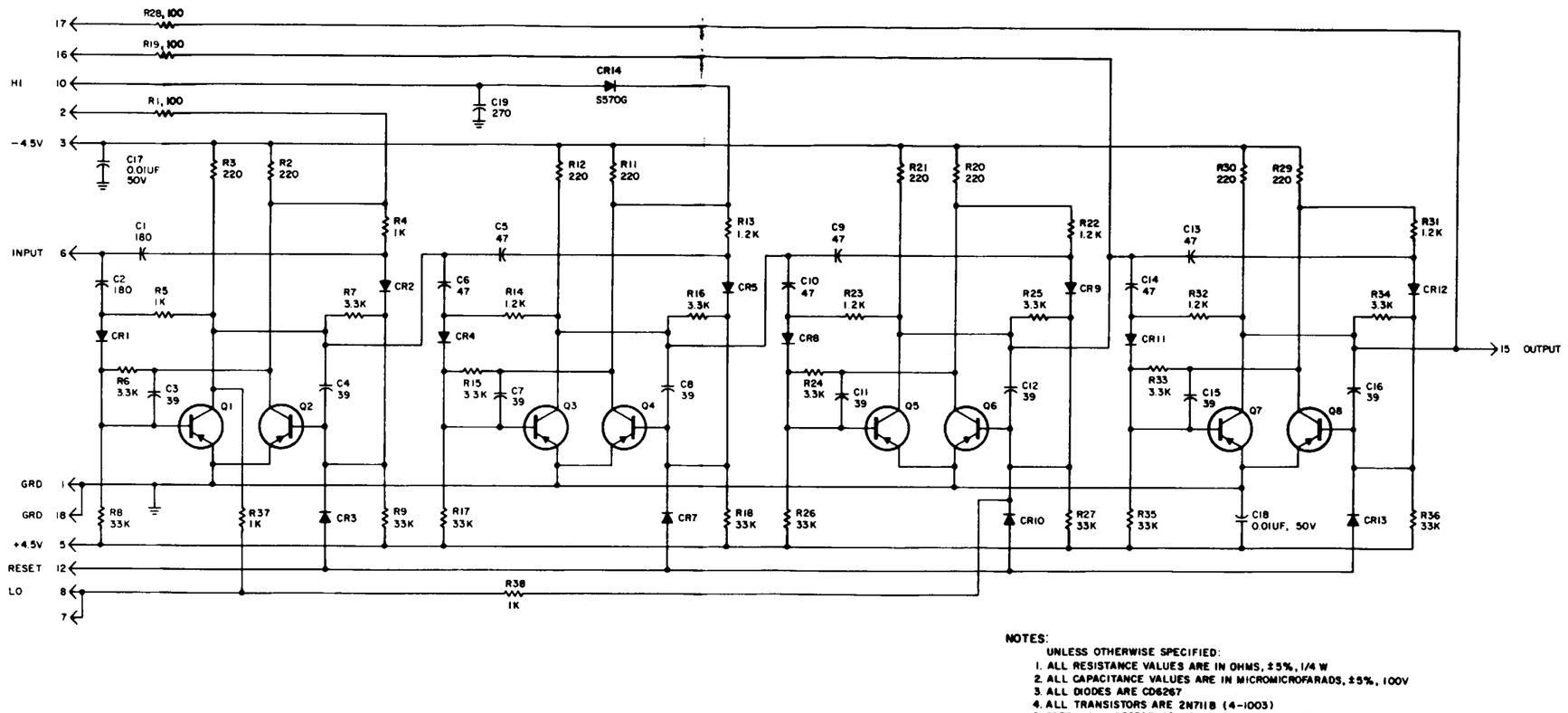
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 500V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE 2N7118 (4-1003)
5. PREFIX ALL REFERENCE DESIGNATIONS WITH A35

Figure 46. Divide-by-16, Schematic Diagram



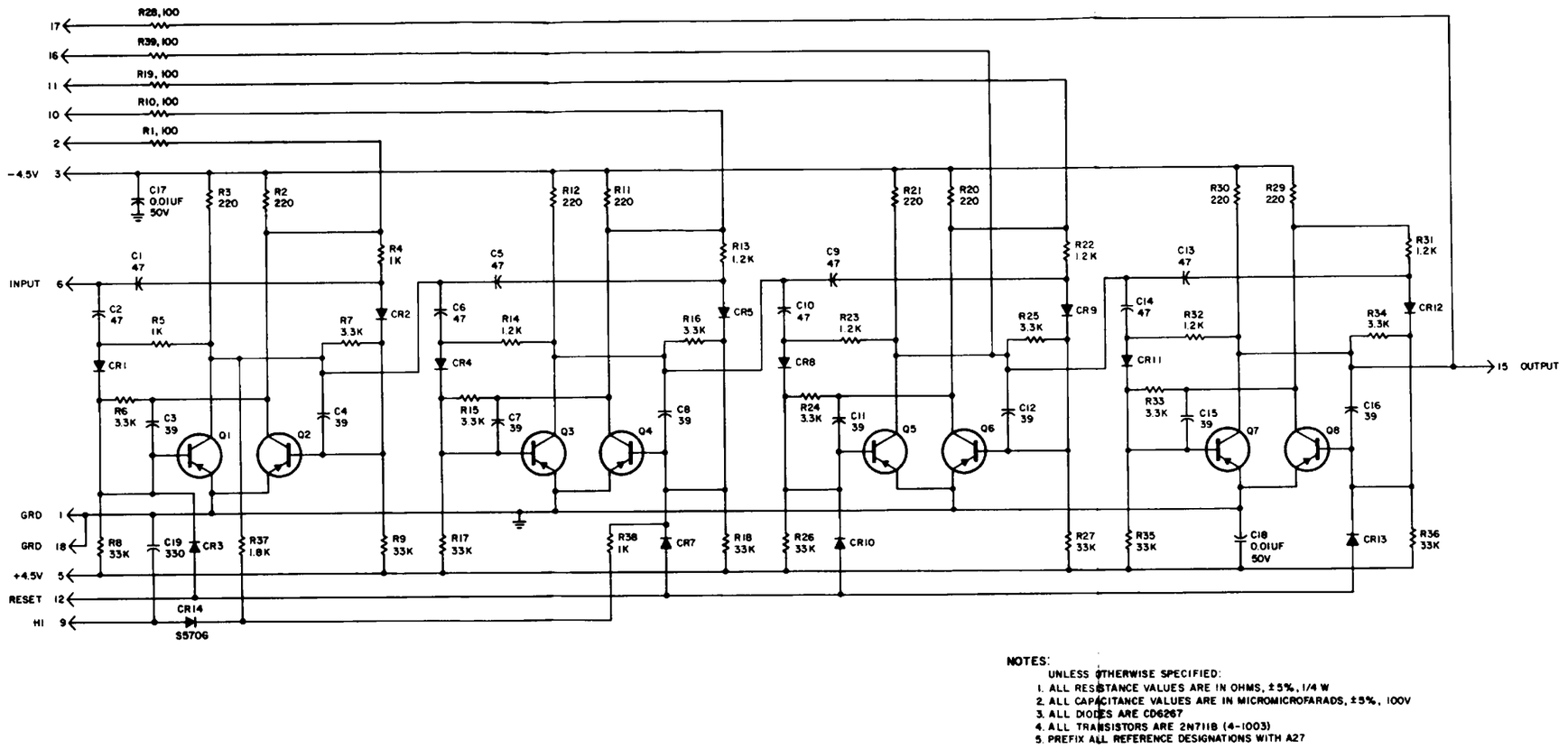
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4 W, ±5%.
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, 500V, ±5%.
3. ALL TRANSISTORS ARE 2N708.
4. PREFIX ALL REFERENCE DESIGNATIONS WITH A33.

Figure 47. Ramp Generator, Schematic Diagram



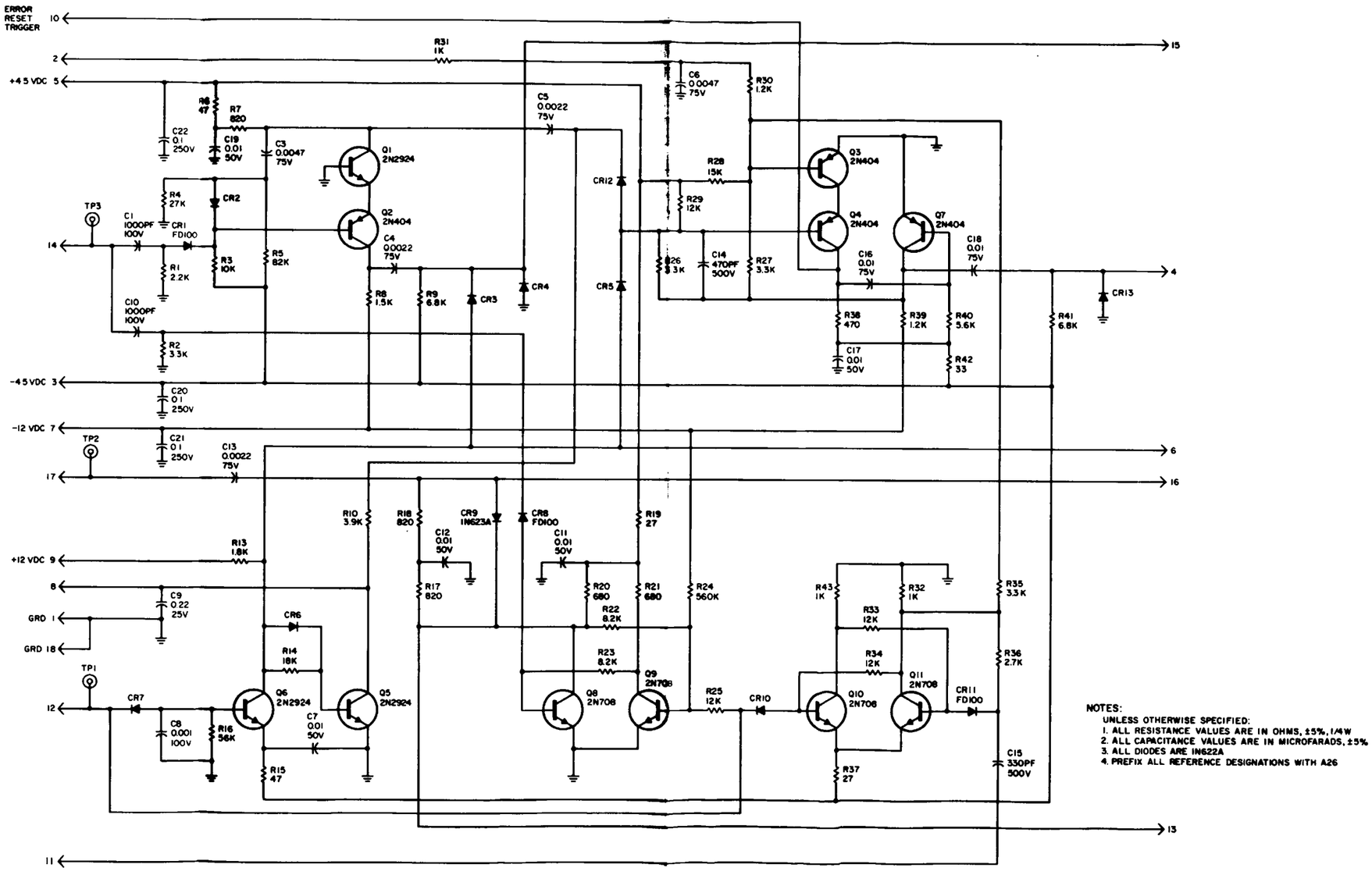
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 100V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE 2N718 (4-1003)
5. PREFIX ALL REFERENCE DESIGNATIONS WITH A25

Figure 48. A Logic, Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4 W
2. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS, ±5%, 100V
3. ALL DIODES ARE CD6267
4. ALL TRANSISTORS ARE 2N711B (4-1003)
5. PREFIX ALL REFERENCE DESIGNATIONS WITH A27

Figure 49. B Logic, Schematic Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, ±5%
3. ALL DIODES ARE IN622A
4. PREFIX ALL REFERENCE DESIGNATIONS WITH A26

Figure 50. Parity Logic, Schematic Diagram

P LOGIC CIRCUIT

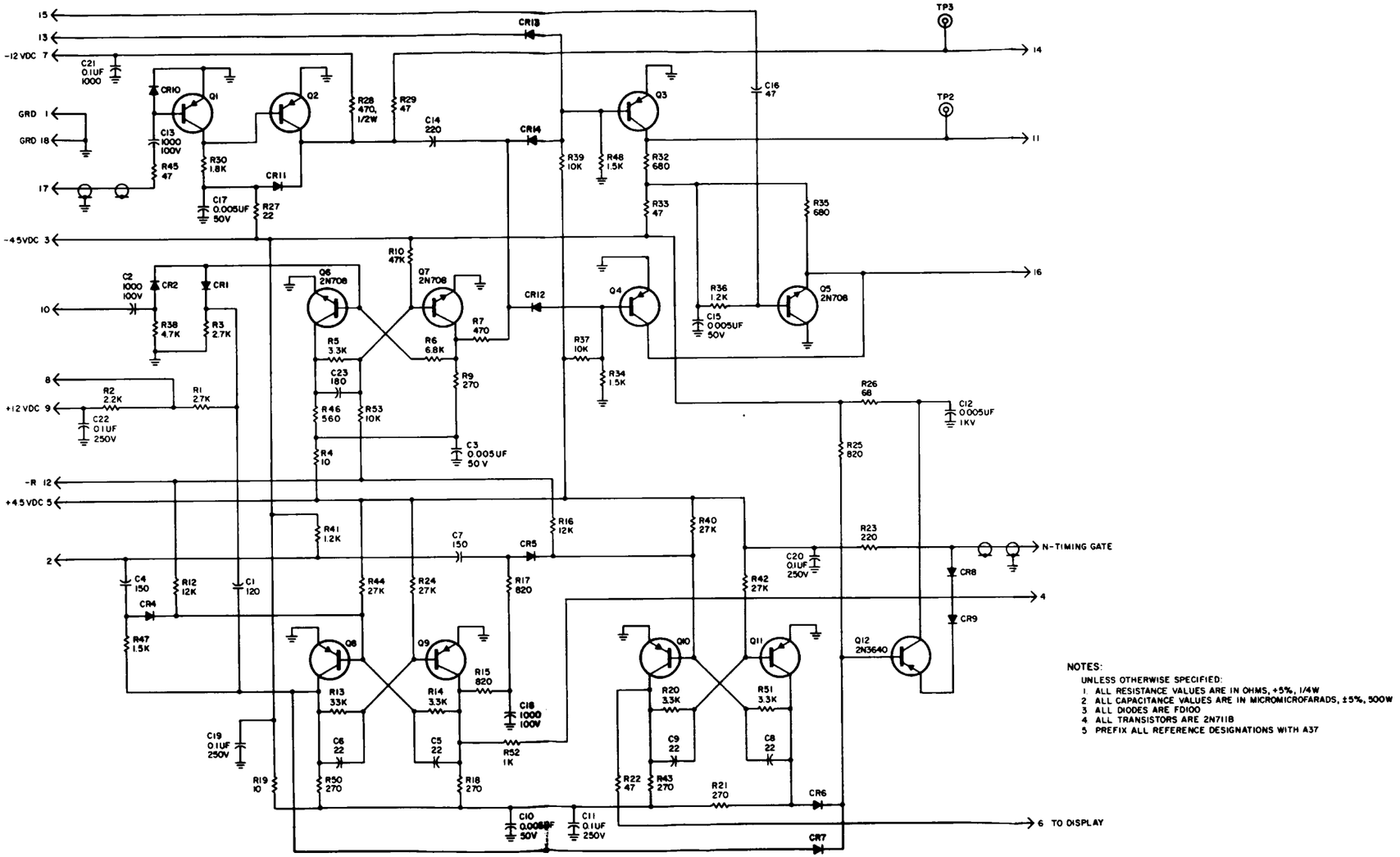


Figure 51. Ratio and Control, Schematic Diagram

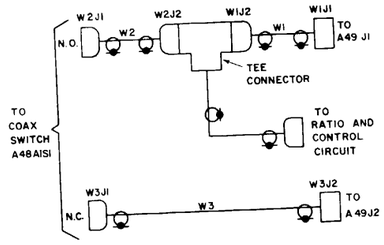


FIGURE 58. COAXIAL SWITCH CABLE ASSEMBLY SCHEMATIC

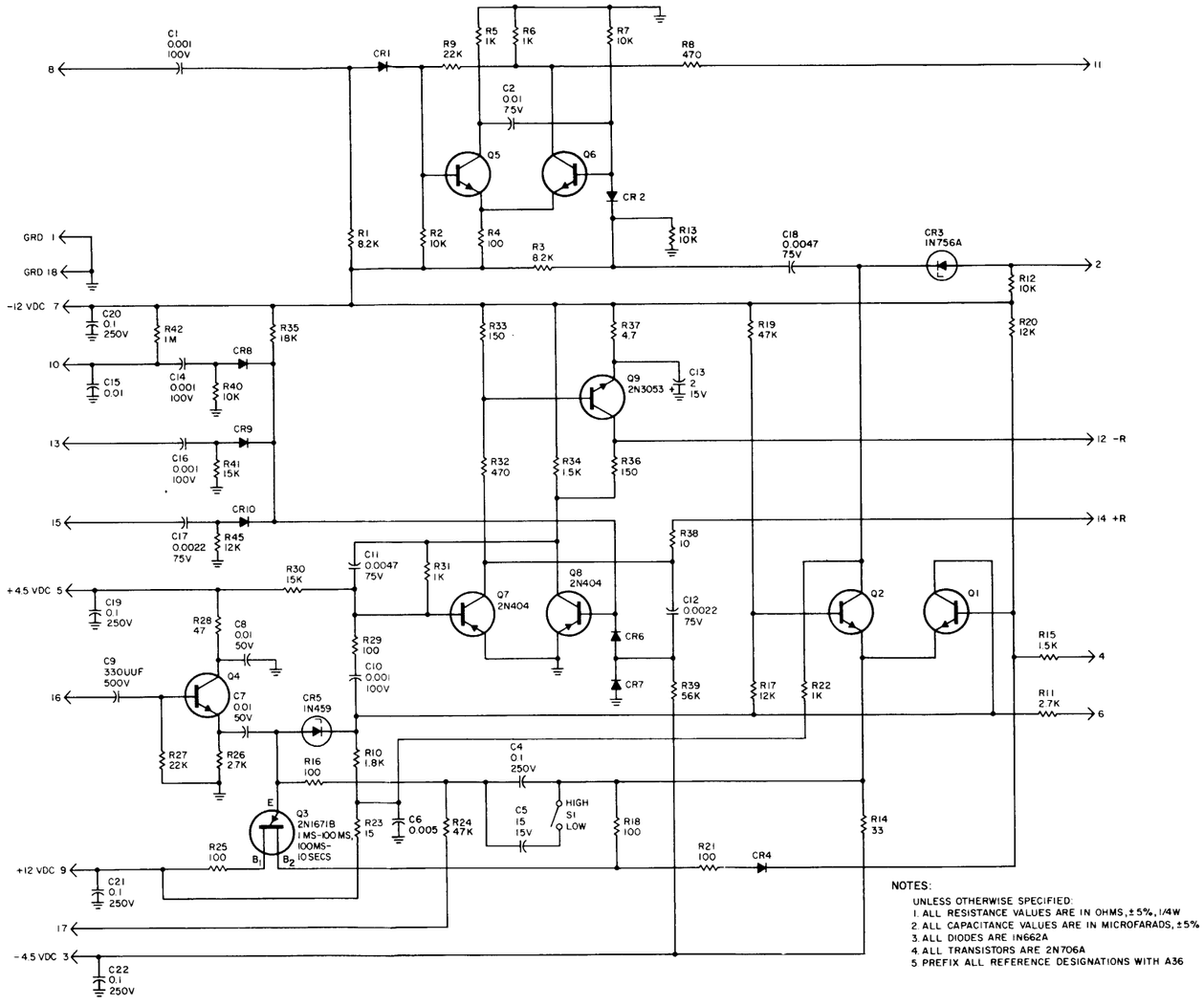


Figure 52. Reset Circuit, Schematic Diagram

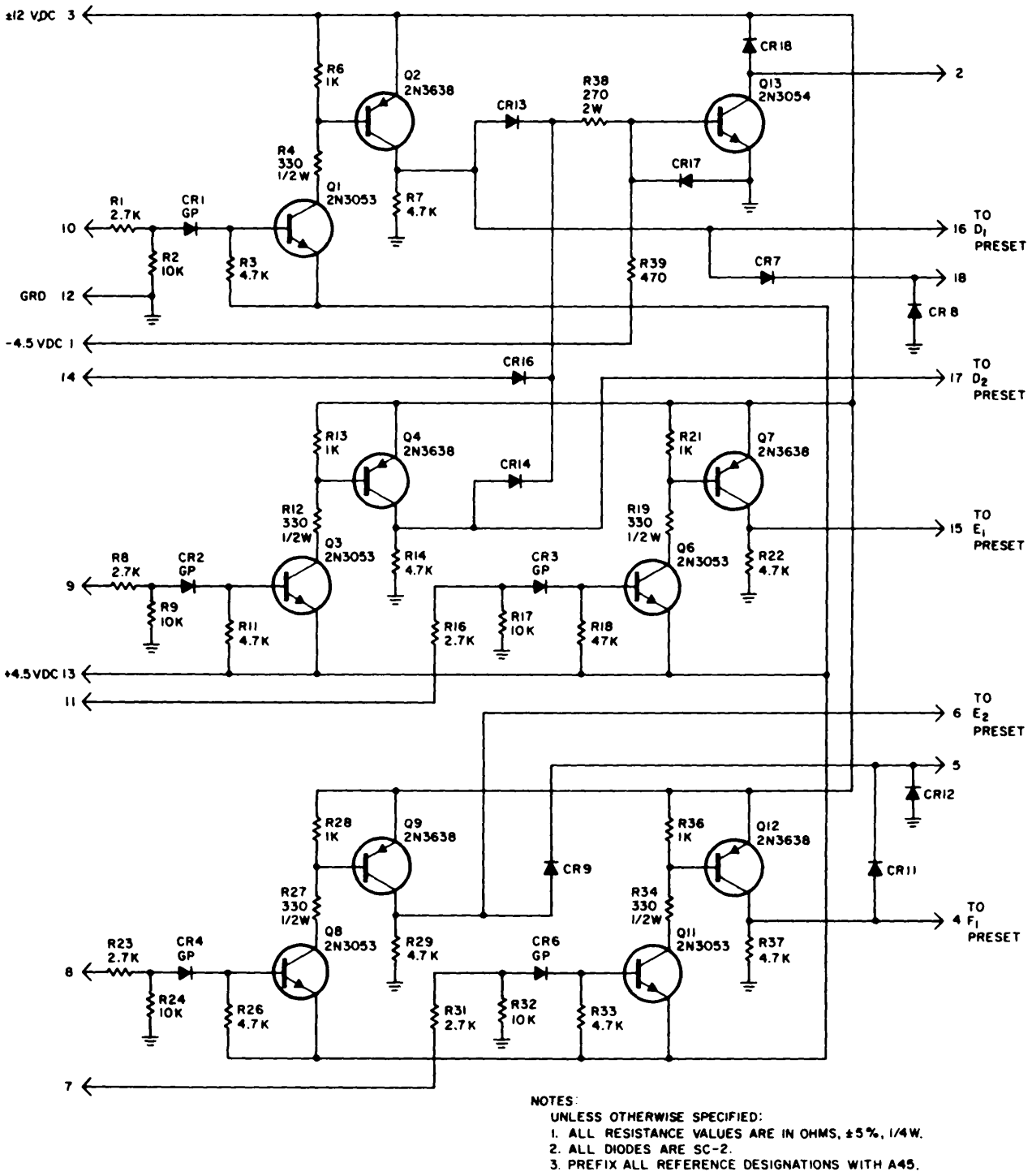
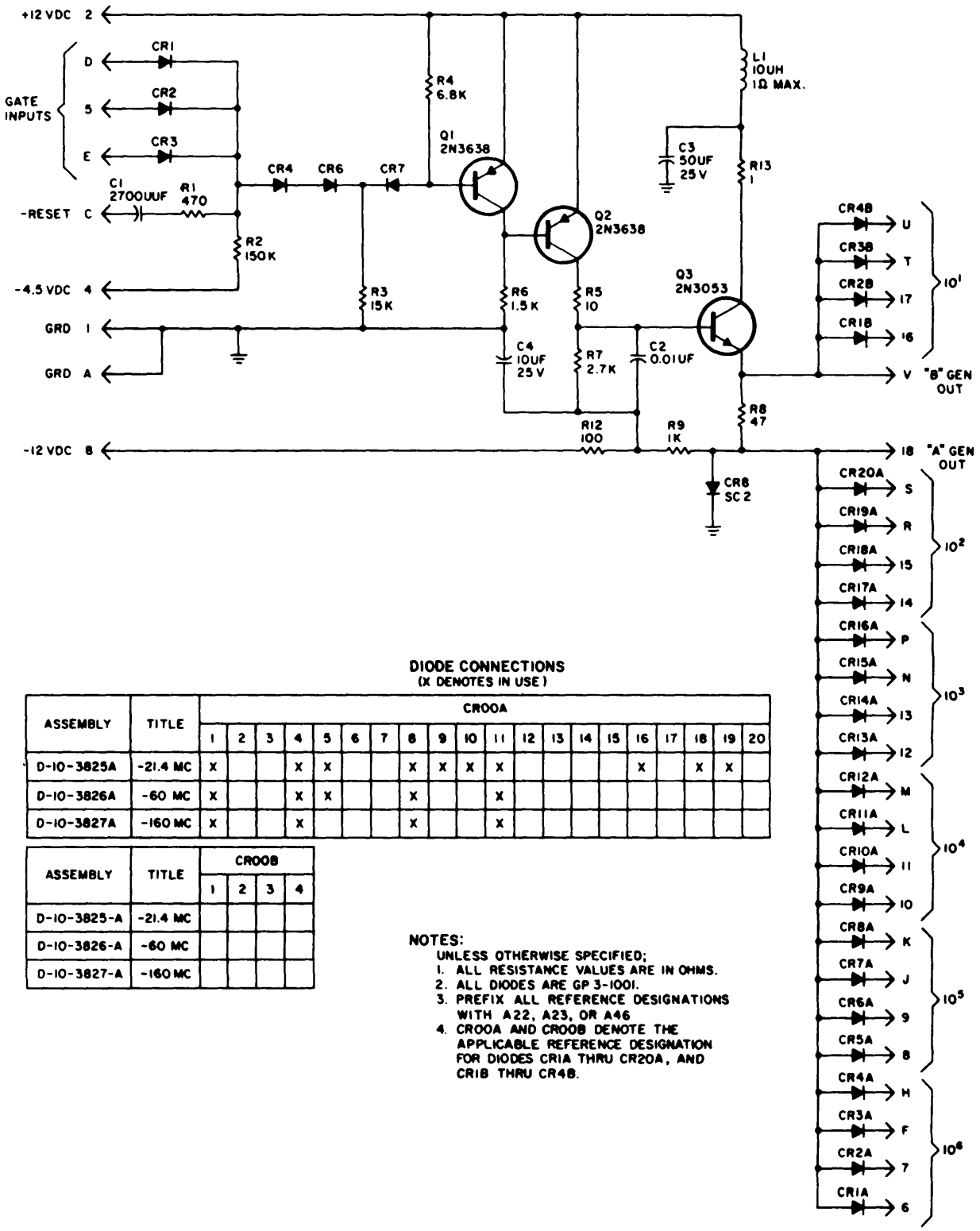


Figure 53. Remote Operation Buffer, Schematic Diagram



DIODE CONNECTIONS
(X DENOTES IN USE)

ASSEMBLY	TITLE	CR00A																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
D-10-3825A	-21.4 MC	X			X	X			X	X	X	X					X		X	X	
D-10-3826A	-60 MC	X			X	X			X			X									
D-10-3827A	-160 MC	X			X				X			X									

ASSEMBLY	TITLE	CR00B			
		1	2	3	4
D-10-3825-A	-21.4 MC				
D-10-3826-A	-60 MC				
D-10-3827-A	-160 MC				

NOTES:
UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTANCE VALUES ARE IN OHMS.
2. ALL DIODES ARE GP 3-1001.
3. PREFIX ALL REFERENCE DESIGNATIONS WITH A22, A23, OR A46
4. CR00A AND CR00B DENOTE THE APPLICABLE REFERENCE DESIGNATION FOR DIODES CR1A THRU CR20A, AND CR1B THRU CR4B.

Figure 54. Preset Generators, Schematic Diagram

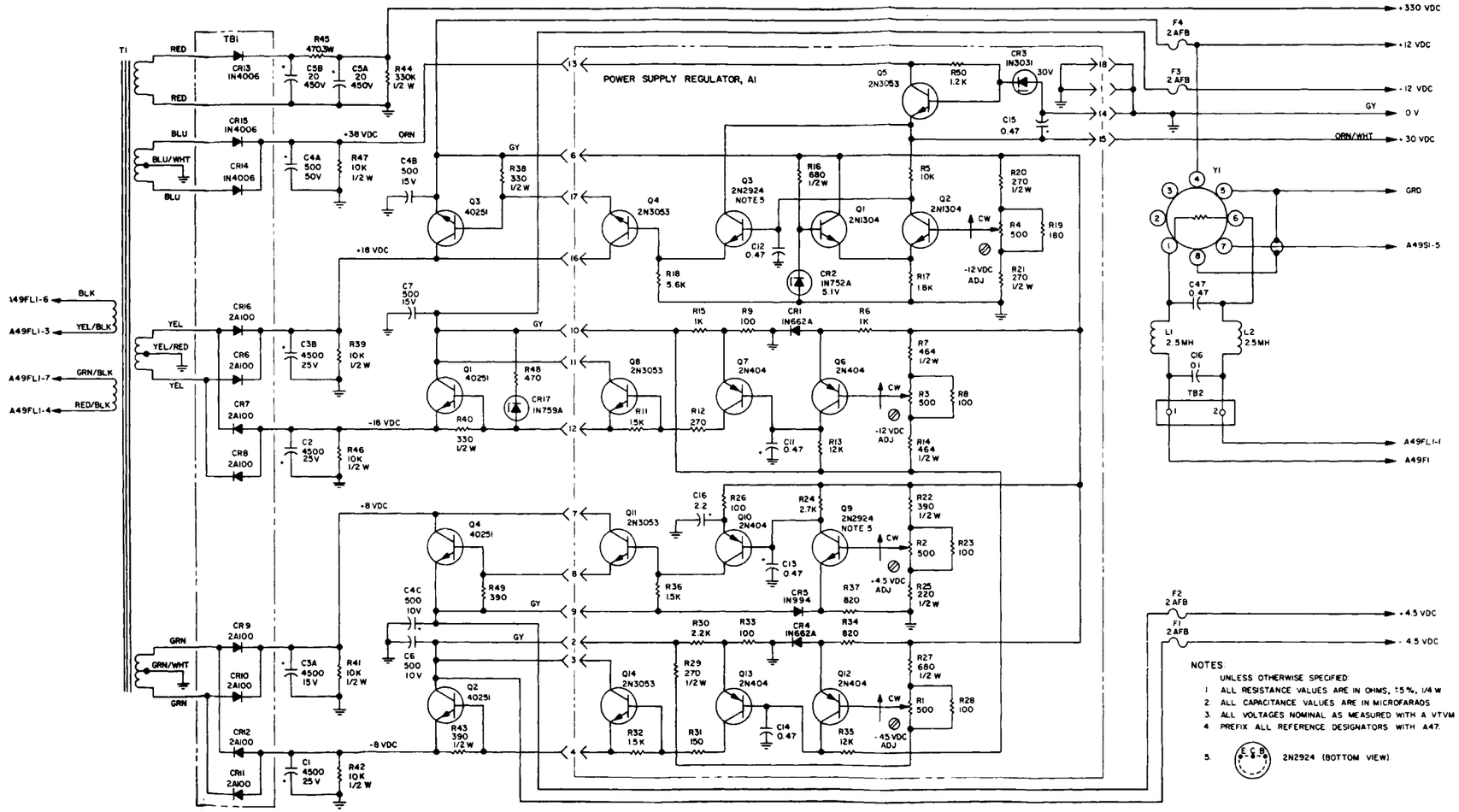


Figure 55. Power Supply, Schematic Diagram

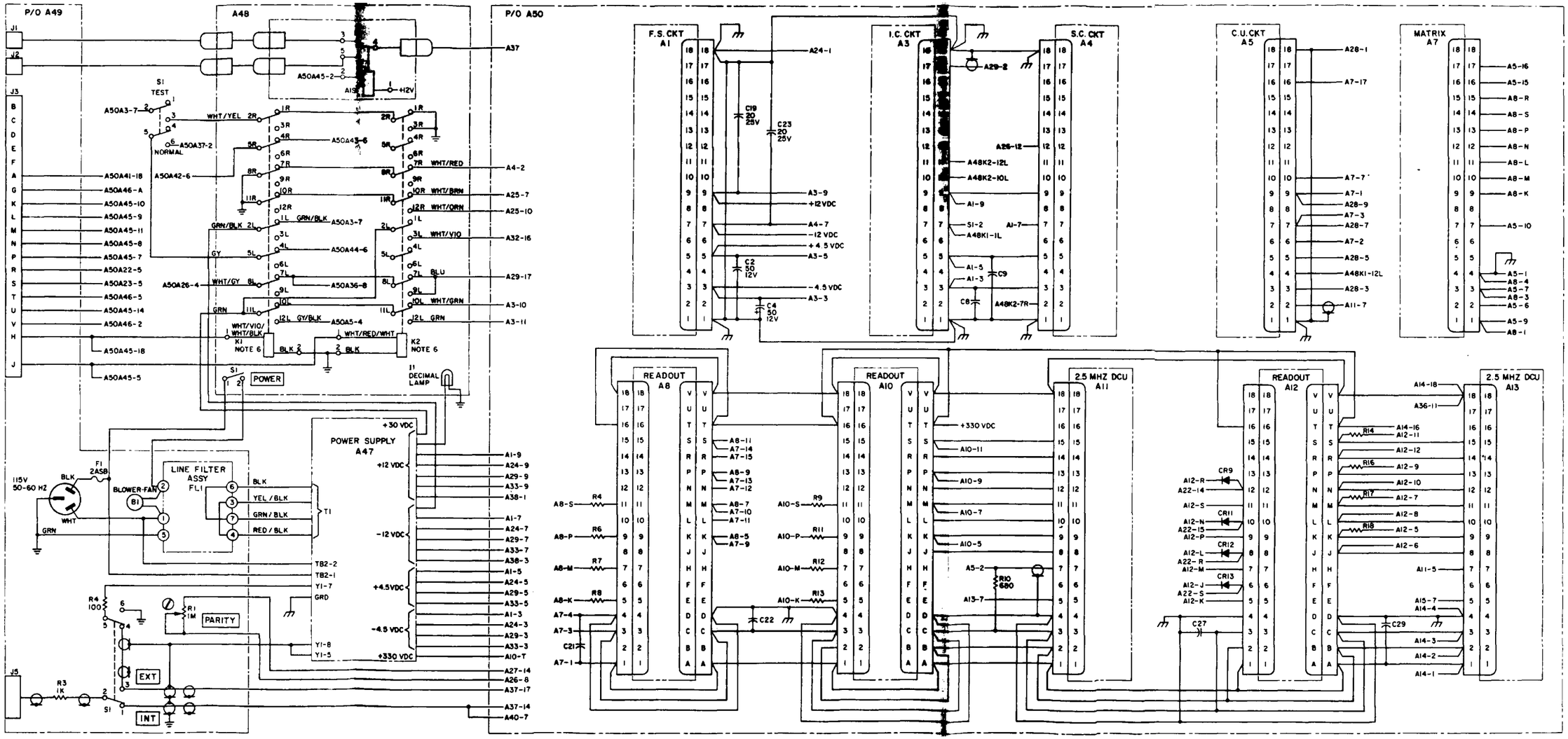


Figure 56. Electronic Counter Interconnection, Wiring Diagram (Sheet 1 of 3)

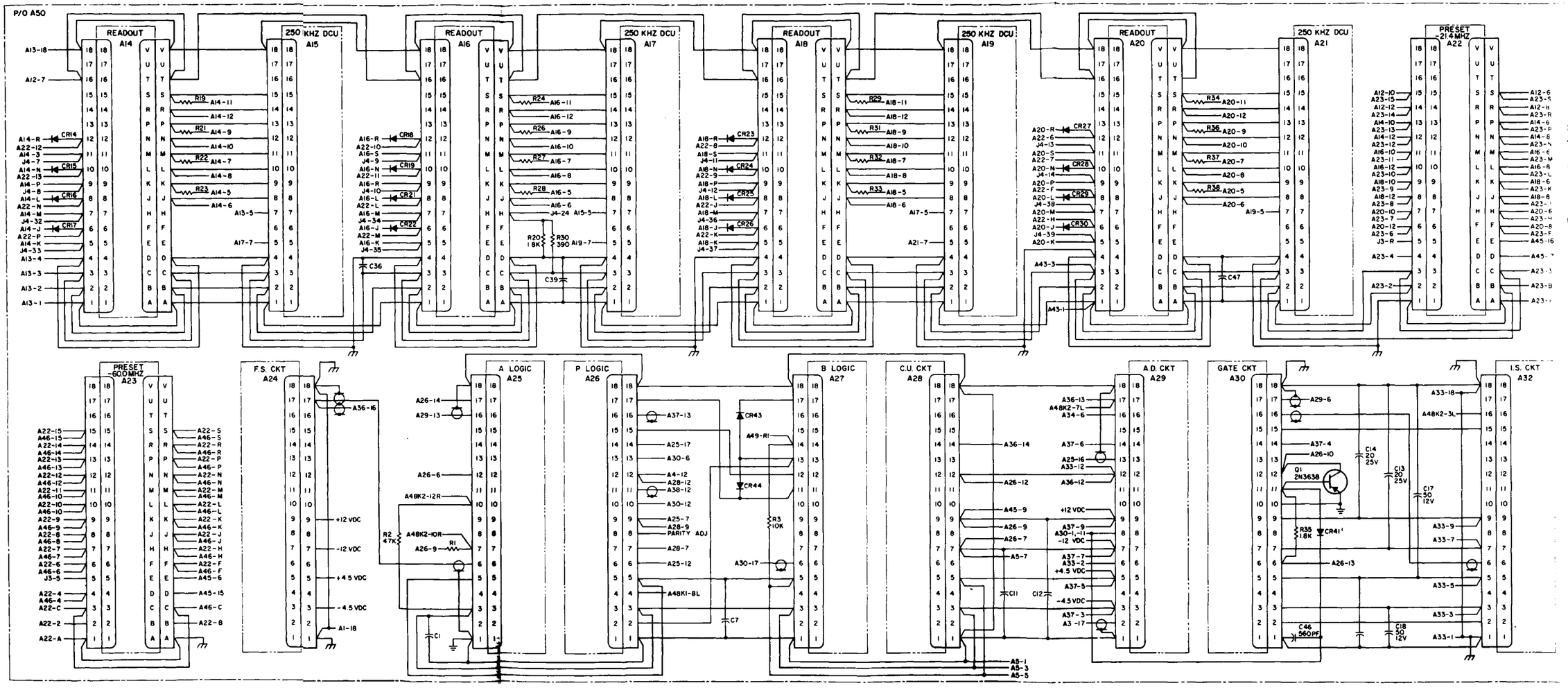
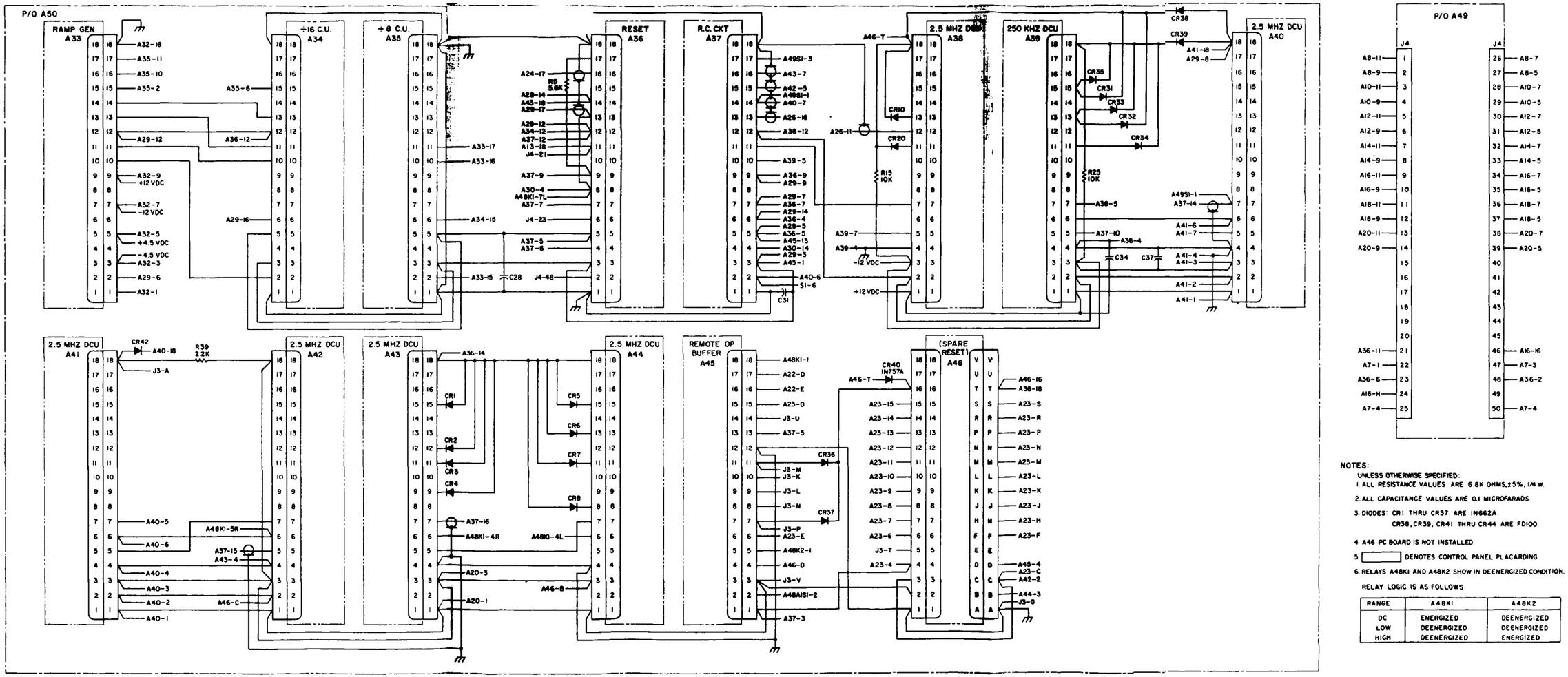


Figure 56. Electronic Counter Interconnection, Wiring Diagram (Sheet 2 of 3)



RANGE	A48K1	A48K2
DC	ENERGIZED	DEENERGIZED
LOW	DEENERGIZED	DEENERGIZED
HIGH	DEENERGIZED	ENERGIZED

Figure 56. Electronic Counter Interconnection, Wiring Diagram (Sheet 3 of 3)

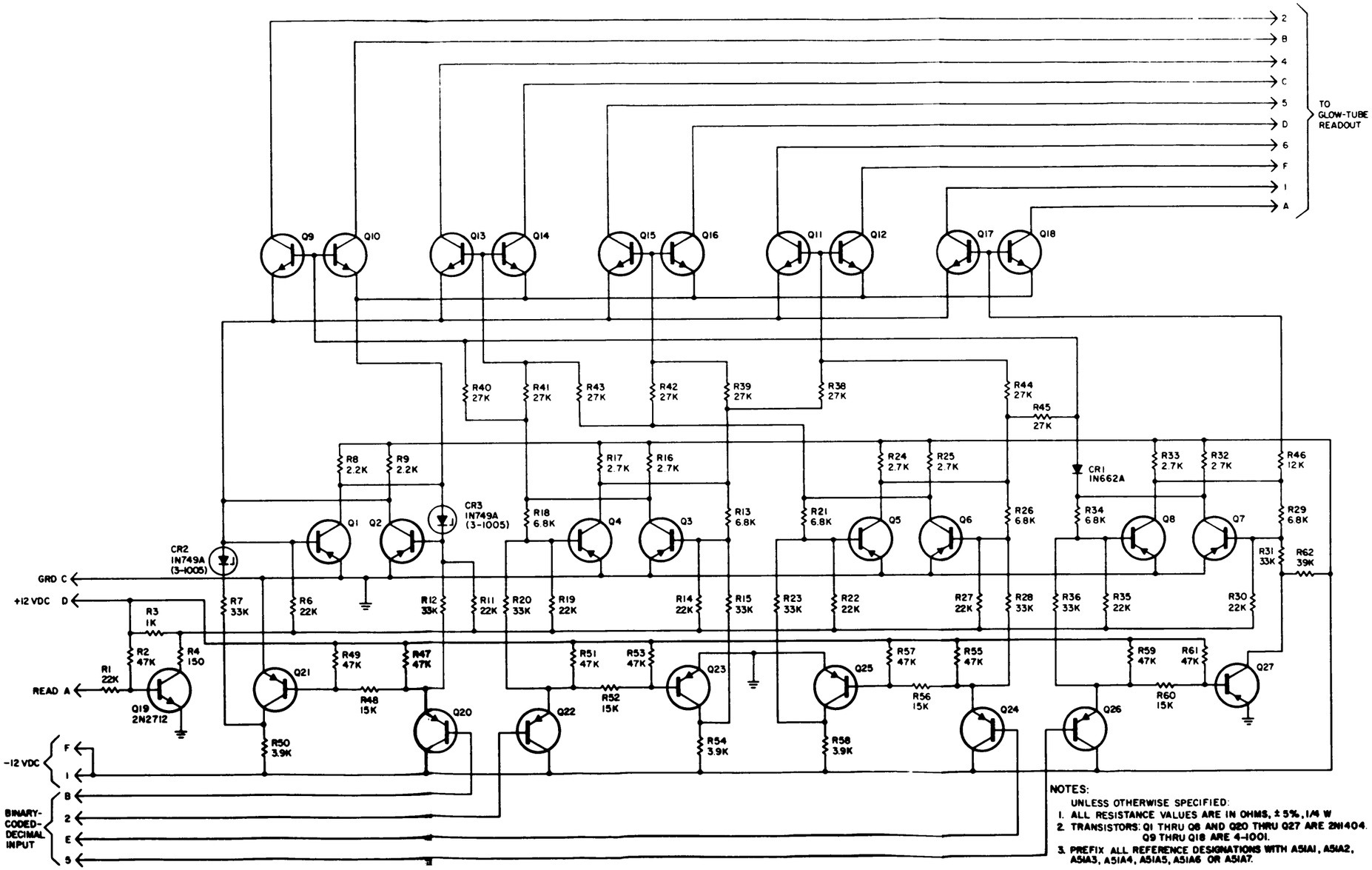


Figure 57. Readout and Decoder, Schematic Diagram

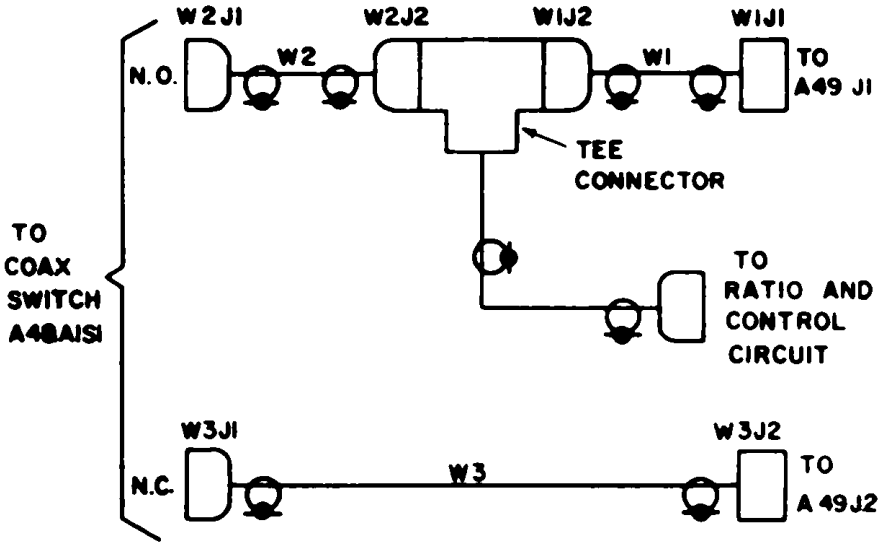


Figure 58. Coaxial Switch Cable Assembly Schematic

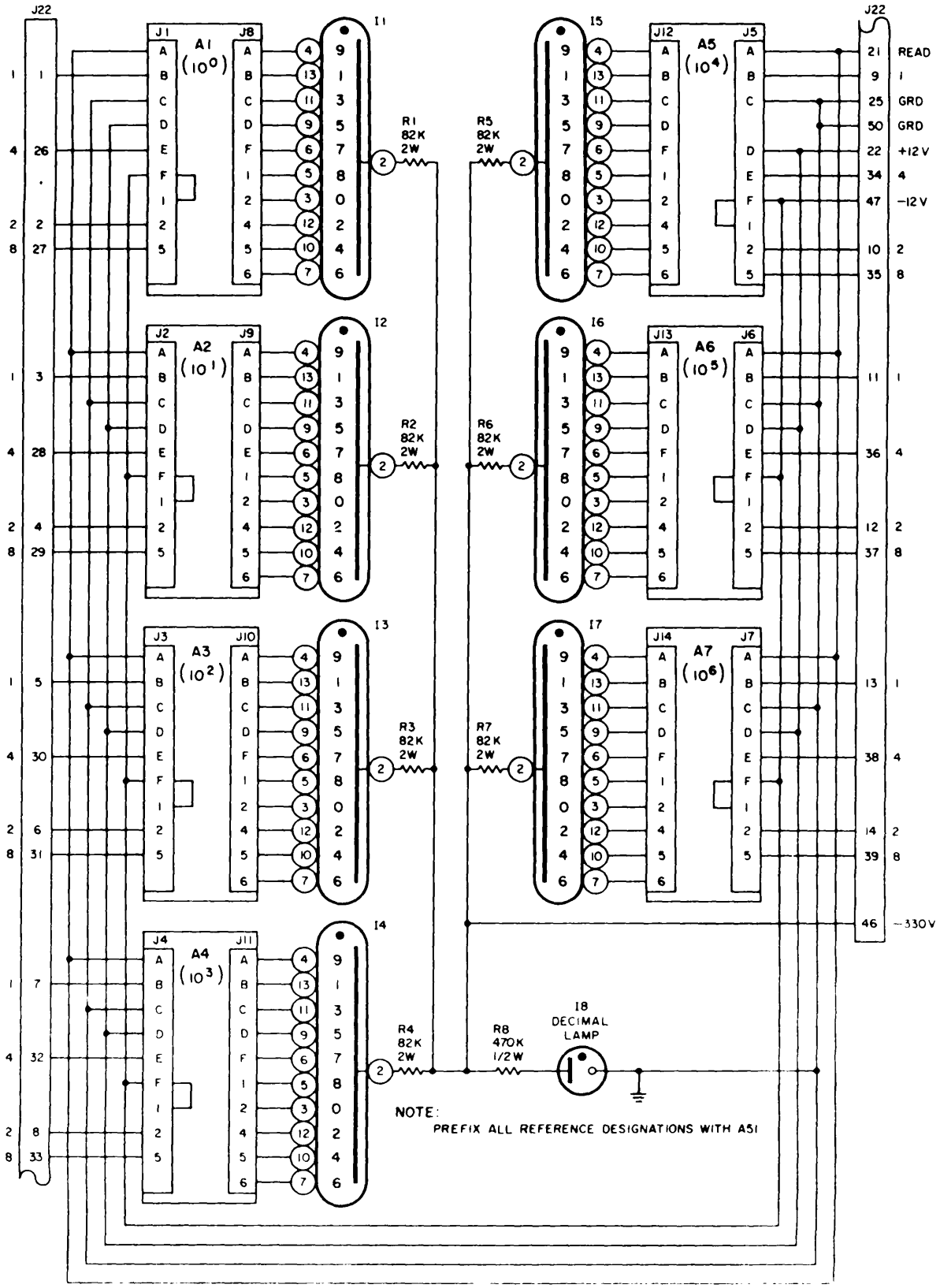


Figure 59. Display Indicator Interconnection Wiring

CHAPTER 6

REPAIRS AND CALIBRATION

Section I. REPAIRS

47. General

This section contains instructions for servicing repairs and adjustments of the electronic counter and display indicator.

48. Parts Replacement Techniques

Caution: Most of the parts of the instrument are removable without any special procedures. The following precautions should be observed.

a. Use a pencil-type soldering iron with a 40-watt maximum capacity. Do not use a soldering gun; damaging voltages can be inducted in components.

b. When soldering transistor leads, solder quickly. Whenever wiring permits, use a heat sink (such as long-nose pliers) between the soldered joint and the transistor. Use approximately the same length and dress of transistor leads as used originally.

c. When installing a shielded wire, reconnect shield to same tie point that it was removed from. Dress all wires in the same manner as removed. Route all wires in the same route as removed. Dress the coaxial cables to fit.

49. Parts Removal and Replacement Procedures

The following steps provide part removal and replacement procedures for the electronic counter and the display indicator.

a. Internal Fuse Replacement. Replacement of internal fuses is accomplished in the following manner:

(1) Remove the top cover as detailed in cover removal procedure, paragraph 56.
(2) Remove the suspected fuse from fuse mounting board on power supply chassis.
(3) Using a multimeter set at the R X 1 resistance range, check for continuity across the fuse.
(4) Continuity greater than 5 ohms will indicate a faulty fuse and will require replacement.

b. Printed Circuit Board Replacement

Caution: The printed circuit boards may have excessively long pigtails on the soldered side of the board. Care should be exercised when removing a board to prevent it from being slammed or scraped against an adjacent board as damage to the adjacent board components may result.

No printed circuit board puller is used to remove boards Simply rock slowly and pull out from socket Be extra careful with the input circuit boards. When removing the double boards (A1 - A24 or A5 - A28), pull the individual board out of the socket, tag cables and disconnect cables from the associated connector, then lift board clear of chassis. Refer to step c for memory readout circuit board removal procedure.

c. Memory Readout Circuit Board Removal The memory readout printed circuit boards requires additional care when removing from the chassis. Remove and replace the boards in the following manner:

(1) Tilt rear end of board (opposite end to where the glow-tube is mounted) first as it is being removed from socket.

(2) Move board toward the rear of the chassis to clear glow-tube from readout housing assembly.

(3) Remove board clear of chassis.

(4) Replacement is the reverse of removal.

(5) Refer to paragraph 19 e for the glow-tube procedures.

d. Display Indicator Readout and Decoder Board Removal and Replacement. The display indicator printed circuit boards are removed in the following manner:

(1) Remove the units top and bottom cover panels.

(2) Remove the single mounting screw on the printed circuit board.

(3) Disconnect the printed circuit board rear socket connector.

(4) Slide the printed circuit board slightly to the chassis rear remove the board from the front socket.

e. Glow-Tube Removal and Replacement. To remove the glow-tubes in the electronic counter, it is first necessary to remove the associated memory readout circuit board. After the boards are removed the glow-tube is pulled from the mounting socket on the board. On the display indicator, remove the instruments front panel mounting screws and allow the readout assembly to clear the chassis. Then gently remove the glow-tubes from the tube socket.

f. Front Panel Removal. The front panel is removed in the following manner.

(1) Remove instruments top and bottom covers as detailed in paragraph 56

(2) Remove screws holding front dress panel and remove POWER switch mounting lock-nut and washer.

(3) Remove plexiglass shield.

(4) Remove orange colored polaroid filter

(5) Remove RFI screen

(6) Remove relay bracelets mounting screws.

g. Front Panel Replacement. The front panel is installed in the following manner.

(1) Mount the relay brackets on the front panel.

(2) Mount the front panel on the chassis frame.

(3) Install the RFI screen in the front panel.

(4) Place the oranged colored poloroid filter over the RFI screen with the front side forward.

Note: To find the front side of the polaroid filter, place it over a shiney surface object. If the shiney surface is still noticeable, the filter is reversed. If the shiney surface is dimmed, this is the frontouter side. Mount it in the panel with the other side against the RFI screen.

(5) Install the plexiglass shield.

(6) Install the front panel on the chassis frame

(7) Install the front dress panel and 4 mounting screws: place the POWER switch in the POWER switch mounting hole and tighten the front panel mounting screws.

(8) Mount the POWER switch and tighten the holding nut.

h. Coaxial Switch Removel and Replacement. The coaxial switch is removed in the following manner.

(1) Remove the instruments front panel as detailed in paragraph f.
(2) Remove printed circuit boards A8 and A10 as detailed in printed circuit board removal paragraph b.
(3) Tag and remove the coaxial switch cable-tee connector.
(4) Tag and disconnect each cable attached to the coaxial switch relay.
(5) Tag and disconnect the control wires to the relay.
(6) Remove the coaxial switch relay bracket mounting screws.
(7) Remove the coaxial switch from the mounting bracket.
(8) Replacement is the reverse of removal.

i. Relay and Relay Socket Removal and Replacement. The two programmer control relays are removed in the following manner.

(1) Remove the front panel as detailed in paragraph f.
(2) Remove the screws holding relay brackets and allow the relay bracket to clear the front panel.
(3) Remove the single screw holding the relay in the relay socket. Remove relay from socket.
(4) Relay replacement is the reverse of removal.

Note: If the relay socket is to be removed, proceed with steps (5) and (6).

(5) Tag and disconnect each wire attached to the relay socket pins.
(6) Replacement is the reverse of removal. Refer to chassis interconnection wiring diagram as necessary for corresponding wire connections.

j. Air Filter Removal and Replacement. The blower fan air filter is removed and replaced by removing the two mounting screws.

k. Blower Fan Removal and Replacement. The blower fan is removed in the following manner.

(1) Remove screws retaining the air filter.
(2) Remove the four mounting screws, retaining the fan assembly.
(3) Tag and disconnect wires to the fan.
(4) Lift fan up, then tilt toward front of the chassis and lift clear of chassis.
(5) Replacement is the reverse of removal.

l. Printed Circuit Board Socket Removal and Replacement. The printed circuit board sockets are removed in the following manner.

(1) Remove the top and bottomcovers to the instrument as detailed in paragraph 46.
(2) Remove the printed circuit board in the socket to be removed.
(3) Remove the printed circuit boards in the adjacent sockets to prevent damage to the printed circuit boards circuit components.

(4) Tag and remove each wire to socket pins; clip any common buss line as required where the printed circuit board sockets are located several sockets in from the end of the common buss line end.

(5) Loosen the socket mounting hardware and remove the damage socket from the chassis.

Note: Several sockets have threaded spacers as mounting nuts. These will require replacement on the same socket after installation of the new socket.

(6) Replacement is the reverse of removal.

m. Removal of Parts from Printed Circuit Boards. The procedure for removal of lead-mounted parts from boards is as follows.

Caution: Excessive heat will damage printed circuit boards. Use a 40-watt soldering iron with a 1/8 inch tip at a temperature not greater than 550 degrees F. Do not apply soldering iron for more than five seconds to any one area. Protect heat-sensitive parts with a heat sink placed between the part and the solder point.

(1) Cut component lead near circuit board or solder weld.
(2) Apply desoldering iron to lead stub.
(3) Remove lead from printed circuit board in the opposite direction it was mounted in.

n. Remounting Parts on Printed Circuit Boards. Replace parts on the assembly printed circuit board in accordance with the following procedure.

(1) Assure minimum clearance of 1/32 inch between part and printed circuit board.
(2) Allow minimum of 1/8 inch between lead bend and body of part.
(3) Adjust clearance between part and printed circuit board with a spacer.
(4) Crimp protruding part leads prior to soldering.
(5) Solder with small-diameter, 60/40 rosin-core solder.
(6) Apply minimum heat that allows free flow of solder.

o. Removal and Replacement of Power-Handling Semiconductor Devices. When replacing power transistors, or high-wattage voltage reference (Zener) diodes, proceed as follows.

(1) Tag and unsolder the leads from the base and emitter terminals of the power transistor or the cathode of the high-reference diode.

(2) Remove attaching screws, insulating sleeves (if used), washer and locking washers, noting their order of assembly so that it may be duplicated when the news power transistor diode is insulating.

(3) Remove the old power-handling device and any mica insulating washer from the heat sink or chassis. Discard the old power-handling device, but save the mica insulating washer for re-use if a new insulating washer is not supplied with the new power-handling device.

(4) Apply thin coating of Silicone Heat Sink Compound, such as Dow Corning No. 340 to mating surfaces of the new power handling device, the mica insulating washer (if used), and the heat sink or chassis.

(5) Install the new power handling device, assembling it and its attaching and insulating hardware to the chassis or heat sink in the order noted during removal of the old device.

(6) Tighten attaching hardware securely and connect and solder leads to the correct terminals of the power handling device. Wipe excess heat sink compound from the edge of the newly-installed power-handling device.

Section II. CALIBRATION

50. General

This paragraph contains calibration procedures for the electronic counter power supply and time-base generator circuits. The accuracy of the instrument circuits is dependent upon the accuracy of the 1-Mc oscillator crystal. Any deviation from the oscillators nominal frequency will insert an error into all frequency measurements. Perform the test set-up procedures as detailed in paragraph 46, removing the electronic counter covers and connect the power cable to a suitable power source.

51. Calibration Procedures

Warning: Be careful when working on the 115-volt ac line connections and the +330 - volt dc circuits. Serious injury or death may result from contact with these ferminals.

Perform the calibration procedures adjustments using voltmeter with a 1 percent (or better) accuracy. If unable to obtain any required indication, perform the trouble- shooting procedures for the malfunctioning circuit.

a. Power Supply Calibration

(1) +12 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for +12 volts dc) between fuse A47F4 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator +12 ADJ control (A47A1R4) for +12 ±0. 12 volts dc.

(2) -12 Volts Dc Circuit Calibration. Connect the voltmeter (adjusted for -12 volts dc) between fuse A47F3 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator -12 ADJ control (A47A1R3) for -12 ±0. 12 volts dc.

(3) +4, 5 Volts DC Circuit Calibration. Connect the voltmeter (adjusted for +4.5 volts dc) between fuse A47F2 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator +4.5 ADJ control (A47A1R2) for +4.5 ±0. 045 volts dc.

(4) -4. 5 Volts DC Circuit Calibration. Connect the voltmeter (adjusted for -4.5 volts dc) between fuse A47F1 and chassis ground. Observe the voltmeter indication and adjust the power supply regulator -4.5 ADJ control (A47A1R1) for -4.5 ±0. 045 volts dc.

b. 1-Mc Oscillator Calibration. Perform the following procedure to calibrate the oscillator crystal.

(1) Set the EXT-INTERNAL switch to INTERNAL position.

(2) Connect the internal 1-Mc oscillator output at connector J3 to the oscilloscope vertical deflection input amplifiers.

(3) Connect a 1 megahertzs frequency standard (10 ppm accuracy) output to the oscilloscope horizontal deflection input amplifiers.

(4) Observe the lissajou pattern displayed on the oscilloscope screen.

(5) Slide the adjustment guard on the top of the 1-Mc oscillator to one side and adjust the oscillator trimmer control until the lissajou pattern stabilizes. If adjustment of the trimmer control fails to stabilize the lissajou pattern, replace the 1-Mc oscillator and repeat the calibration procedure.

CHAPTER 7

SHIPMENT, LIMITED STORAGE, AND DEMOLITION TO PREVENT ENEMY USE

Section I SHIPMENT AND LIMITED STORAGE

52. Disassembly of Equipment

Prepare the electronic counter for shipment and storage as follows.

a. Disconnect all leads and power cable.

b. Remove the unit for the mounting rack

c. Assemble all units at convenient area for packaging.

53. Repackaging for Shipment or Limited Storage

a. Material Requirements. If the original shipping cartons are not available, the following materials are required for packaging the display indicator For stock numbers of materials refer to SB 38-100, Preservation, Packaging, and Packing Materials, Supplies, and Equipment used by the Army.

Material	Quantity
Barrier material, waterproof	30 sq ft
Tape, cloth backing, waterproof	30 ft
Twine cotton	10 ft
Fiberboard, corrugated	30 sq ft
Tape, gummed paper	25 ft
Cushioning material	36 sq ft

b. Packaging. Package the items of the electronic counter outlined below.

(1) Electronic counter. Cushion the electronic counter on all surfaces with a pads of cushioning material. Place the cushioned unit within a wrap of corrugated fiberboard. Secure the wrap with gummed tape.
(2) Digital Display Indicator. Cushion the display indicator on all surfaces with pads of cushioning material. Place the cushioned unit within a wrap of corrugated fiberboard. Secure the wrap with gummed tape.
(3) Miscellaneous items. Wind each cable assembly into a coil and tie with cotton twine. Package the connectors and adapters to insure protection. Use cushioning material to cushion each item as required. Consolidate the miscellaneous items within a wrap of corrugated fiberboard.

c. Packing. Pack each of the consolidated packages in separate, nailed, wooden boxes: the electronic counter and minor items in box 1 or 2, and the display indicator box 2 of 2.

Section II. DEMOLITION OF MATERIAL TO PREVENT ENEMY USE

54. Authority For Demolition

The demolition procedures given in paragraph 55 will be used to prevent the enemy from using or salvaging this equipment. Demolition of the equipment will be accomplished only upon the order of the commander.

55. Methods of Destruction

The tactical situation and time available will determine the method to be used when destruction of equipment is ordered. In most cases, it is preferable to demolish completely some portions of the equipment rather than partially destroy all the equipment units.

a. Smash. Use sledges, axes, hammers, crowbars, and any other heavy tools available to smash the interior units of the set.

(1) Use the heaviest tool on hand to smash the connectors, display indicators, knobs, and

Note: Heavy tools will effectively destroy the external parts mentioned in (1) above, but the remainder of the exposed surfaces of the equipment are constructed of steel plate; attempts to damage it by smashing will be useless.

(2) Remove the chassis from the cabinet. With a heavy hammer or bar, smash as many of the exposed parts of the various chassis as possible.

b. Cut. Use axes, handaxes, machetes, and similar tools to cut cabling, cording, and wiring. Use a heavy axe or machete to cut the power cable. Cut all cords and cables in a number of places.

Warning: Be extremely careful with explosives and incendiary devices. Use these items only when the need is urgent.

c. Burn. Burn the technical manuals first. Burn as much of the equipment as is flammable; use gasoline, oil, flamethrowers, and similar materials. Pour gasoline on the cut cables and internal wiring and ignite it. Use a flamethrower to burn spare parts or pour gasoline on the spares and ignite them. Use incendiary grenades to complete the destruction of the unit.

d. Explode. Use explosives to complete demolition or to cause maximum damage, before burning, when time does not permit complete demolition by other means. Powder charges, fragmentation grenades, or incendiary grenades may be used. Incendiary grenades usually are more effective if destruction of small parts and wiring is desired.

(1) Use a fragmentation grenade to destroy the interior of the display indicator. Remove the outer cabinet, turn chassis over on ground while propping up one end and toss grenade under chassis and stand clear.

(2) Smash any printed circuit board which may remain intact.

(3) For quick destruction of the display indicator, place an incendiary grenade on top of the unit. Get away from the unit after the grenade is placed.

e. Dispose. Bury or scatter destroyed parts or throw then into nearby waterways. This is particularly important if a number of parts have not been completely destroyed.

APPENDIX I

MAINTENANCE ALLOCATION CHART

FOR

COUNT, ELECTRONIC, DIGITAL READOUT, ID-1341/GR

AND

INDICATOR, DIGITAL DISPLAY, ELECTRONIC, ID-1342/GR

MAINTENANCE ALLOCATION

SECTION I

INTRODUCTION

1. General. This document allocates to the lowest appropriate level the maintenance functions to be performed on components, assemblies and subassemblies of equipment managed by USASA. Also specified are the special tools and other equipment required at each level to perform the assigned maintenance functions.

2. Format of Maintenance Allocation Chart. The Maintenance Allocation Chart is divided into five columns. The function of each column and the entries appropriate thereto are discussed below:

a. Component. In column (1) is entered only the nomenclature (JEMDS) or commercial item name. Additional descriptive data are included only where clarification is necessary to identify the component. The listing of components, assemblies, and subassemblies is normally in top-down order; that is, assemblies which are Part of a component are listed immediately below that component and subassemblies which are Part of an assembly are listed immediately below that assembly.

b. Maintenance Function. The various functions allocated to maintenance levels are cited in column (2). In all, the ten functions defined below are specified.

(1) Service. Clean, preserve, and replenish lubricants.

(2) Adjust. Regulate periodically to prevent malfunction.

(3) Inspect. Verify serviceability and detect incipient electrical or mechanical failure by scrutiny.

(4) Test. Verify serviceability and detect incipient electrical or mechanical failure by use o-f special equipment such as gauges and meters.

(5) Replace. Substitute serviceable components, assemblies or subassemblies for unserviceable components, assemblies or subassemblies.

(6) Repair. Restore an item to serviceable condition through correction of a specific failure or unserviceable condition. (This function includes -- but is not limited to -- welding, grinding,

riveting, straightening, and replacement of Parts other than those replaced by the trial-and-error technique from running-spares stock such as fuses, lamps, or electron tubes.

(7) Align. Adjust components of an electrical system so that functions are properly synchronized.

(8) Calibrate. Determine, check, or rectify the graduation of a system, components of a system, or an instrument.

(9) Overhaul. Restore an item to COMPLETELY SERVICEABLE condition as prescribed by serviceability standards. (This function is accomplished through employment of the Inspect and Repair Only as Necessary (IROAN) technique. Maximum utilization of diagnostic equip- ment is combined with minimum disassembly of the item during the overhaul process.)

(10) Rebuild. Restore an item to a standard as near as possible to original or new condition in appearance, performance, and life expectancy. (This function is accomplished by complete disassembly of the item, inspection of all Parts or components, repair or replacement of worn or unserviceable elements using original manufacturing tolerances and/or specifications, and subsequent reassembly.)

c. Level of Maintenance. A symbol placed in one or more of the 5 subcolumns of column (3) indicates responsibility for performance of that Particular level of maintenance. (This entry does not necessarily indicate that repair Parts will be stocked at that level specified.) Any level of maintenance higher than that cited by the symbol is authorized to perform the indicated operation.

d. Tools Required. In column (4) are listed the codes assigned to the individual tool and test and maintenance equipment referenced in Section III. The group of codes in this column indicates the special tool, test, and maintenance equipment normally required to perform the associated function in column (2). Appropriate substitutions may be made; in the case of electrical instruments, the sensitivity of the replacement must be equal to or greater than that for which the substitution was made.

e. Remarks. Entries may be made in column (5) to amplify on those made in other columns.

3. Maintenance by Using Organization. USASA organizations will perform the category of maintenance authorized. Direct Support maintenance will normally be performed by tactical units; General Support maintenance will normally be performed by fixed facilities.

4. Furniture and Mounting Hardware. The basic entries of the Maintenance Allocation Charts do not include furniture or mounting hardware such as chairs, typewriters, ashtrays, screws, nuts, bolts, washers, brackets, and clamps.

5. Comments. Comments concerning omissions and discrepancies in this appendix will be prepared on DA Form 2028 and forwarded directly to Commanding Officer, US Army Security Agency Materiel Support Command, ATTN: IAMME/M, Vint Hill Farms Station, Warrenton, Virginia 22186.

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A1 FS Ckt. (Proprietary) Eldorado Part # 10-3417	INSPECT TEST REPLACE REPAIR		+ 	 	 + + 	 	 1 	 Factory Repair Required
1A2 Not Used								
1A3 IC Ckt (Proprietary) Eldorado Part #10-3955 Printed Ckt Board	TEST REPLACE REPAIR					+ + 	2	Factory Repair Required
1A4 SC Ckt (Proprietary) Eldorado Part #10-34524 Printed Ckt Board	INSPECT TEST REPLACE REPAIR		+ 	 + + 	 	 	 2 	 Factory Repair Required
1A5 CU Ckt. (Proprietary) Eldorado Part #10-3416	INSPECT TEST REPLACE REPAIR		+ 	 + + 	 	 	 2 	 Test by Replacement Only Factory Repair Required
1A6 Not Used								
1A7 Matrix Eldorado Part #10-3423 Printed Ckt Board	INSPECT TEST REPLACE REPAIR		+ 	 + + 	 +	 	 7 7	 Test by Replacement Only Factory Repair Required

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A8 Readout Eldorado Part #10-1988 Printed Ckt Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A9 Not Used								
1A10 Readout Eldorado Part #10-1988 Same as 1A8. Printed Ckt Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A11 25 MC DCU Eldorado Part #10-3968 Printed Circuit Board	INSPECT		+					
	TEST			+			2 & 7	
	REPLACE				+			
	REPAIR				+		2 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A12 Readout Eldorado Part #10-1988 Same as 1A8. Printed Ckt Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A13 2.5 MC DCU. Eldorado Part #10-3967. Printed Ckt. Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A14 Readout Eldorado Part #10-1988. PC Board. Same as 1A8	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A15 250KC DCU. Eldorado Part #10-3966. PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A14 Readout Eldorado Part #10-1988. PC Board. Same as 1A8	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A17 250KC DCU Eldorado Part #10-3966. PC Board. Same as 1A15	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A18 Readout Eldorado Part #10-1988. PC Board. Same as 1A8	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A19 250KC DCU Eldorado Part #10-3966. PC Board. Same as 1A15	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A20 Readout Eldorado Part #10-1988. PC Board. Same as 1A8.	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A21 250KC DCU Eldorado Part #10-3966. PC Board. Same as 1A15	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A22 Preset (-21.4 MHz) Eldorado Part #10-3825. PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A23 Preset (-60.0 MHz) Eldorado Part #10-3826. PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A25 A Logic Eldorado Part #10-3414. PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A26 P Logic Eldorado Part #10-3418. PC Board w/test points	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR					+	1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A27 B Logic Eldorado Part #10-3415. PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A29 AD Ckt. Eldorado Part #10-3420. Printed Ckt Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR					+	1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A30 Gate Ckt (Proprietary) Eldorado Part #10-4022. Printed Ckt Board	INSPECT		+					
	TEST					+	1	
	REPLACE					+		
1A31 Not Used								

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A32 IS Ckt (Proprietary) Eldorado Part #10-3422 Printed Ckt Board	TEST REPLACE					+ +	1	Sealed Unit
1A33 R Generator Ckt Eldorado Part # 10-3496. Printed Ckt Board	INSPECT TEST REPLACE REPAIR OVERHAUL REBUILD		+ 	 + + 	 	 + + +	 1 & 7 1 & 7 	
1A34 ÷16CU Eldorado Part #10-3412 Printed Ckt Board w/test points and cable connectors	INSPECT TEST REPLACE REPAIR OVERHAUL REBUILD		+ 	 + + 	 	 + + +	 2 & 7 	
1A35 ÷ 8CU Eldorado Part #10-3413. Printed Ckt Board	INSPECT TEST REPLACE REPAIR OVERHAUL REBUILD		+ 	 + + 	 	 + + +	 1 & 7 1 & 7 	
1A36 Reset Ckt. Eldorado Part #10-3419. Printed Ckt Board w/two position switch	INSPECT TEST REPLACE REPAIR OVERHAUL REBUILD		+ 	 + + 	 + 	 + +	 1 & 7 1 & 7 	

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A37 RC Ckt. Eldorado Part #10-3421. Printed Ckt Board w/test points & RF cable connector	INSPECT		+					
	TEST			+			2 & 7	
	REPLACE			+				
	REPAIR					+	2 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A38 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board. Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A39 250 KC DCU Eldorado Part #10-3966. Printed Ckt Board Same as 1A15	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A40 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A41 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board. Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A42 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A43 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A44 2.5 MC DCU Eldorado Part #10-3967. Printed Ckt Board Same as 1A13	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A45 Remote Operation Buffer, Eldorado Part #10-3807	INSPECT		+					
	TEST			+			7	
	REPLACE			+				
	REPAIR				+		7	
	OVERHAUL					+		
	REBUILD					+		
1A46 Not Used								

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A47 Power Supply Subassembly Eldorado Part #10-3843	INSPECT		+					
	TEST		+				7	
	REPAIR				+		7	
	CALIBRATE			+			7	
	OVERHAUL					+		
	REBUILD					+		
1A47A1 Voltage Regulator Circuit Board. Printed Ckt Board. Eldorado Part #10-3426	INSPECT		+					
	TEST			+			7	
	REPLACE			+				
	REPAIR				+		7	
	CALIBRATE			+			7	Calibrate only as Part of 1A47
	OVERHAUL					+		
	REBUILD					+		
1A48 Front panel w/3 relays as piece parts	INSPECT		+					
	TEST		+				7	
	REPAIR			+				
1A48A1 Power Divider Relay Assembly Eldorado Part #10-3881	INSPECT		+					
	TEST				+		3, 4, 5, 6, 7	
	REPLACE				+			
1A49 Rear panel assembly w/cooling fan & line filter	INSPECT		+					
	TEST			+			7	Line filter & fan are considered piece Parts
	REPAIR			+			7	

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A50 Logic Chassis Assembly	SERVICE							Bus volt and Output
	INSPECT		+					
	TEST		+				7	
	REPAIR			+			7	
1A51 Indicator, ID-ID-1342, remote readout unit (410 Slave) consists of 7 PC Boards w/nixie tubes as subassemblies	INSPECT	+						
	REPLACE		+					Replace Nixies
	REPAIR		+					
	OVERHAUL					+		
	REBUILD					+		
1A51A1 Readout Decoder Eldorado Part #10-3790 PC Board	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A51A2 Readout Decoder Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A51A3 Readout Decoder Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

(1) PART OR COMPONENT	(2) MAINTENANCE FUNCTION	(3) LEVEL OF MAINTENANCE					(4) TOOLS REQUIRED	REMARKS
		ORG		DIR	GEN			
		OP 1	MECH 2	SPT 3	SPT 4	DEP 5		
1A51A4 Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A51A5 Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A51A6 Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		
1A51A7 Eldorado Part #10-3790 PC Board Same as 1A51A1	INSPECT		+					
	TEST			+			1 & 7	
	REPLACE			+				
	REPAIR				+		1 & 7	
	OVERHAUL					+		
	REBUILD					+		

SECTION III
ALLOCATION OF TOOLS FOR MAINTENANCE FUNCTIONS

Counter, ID-1341/GR and
Indicator, ID-1342/GR

	ORG		DIR	GEN		TOOL	
	OP 1	MECH 2	SPT 3	SPT 4	DEP 5	CODE	REMARKS
Oscilloscope, AN/USM-140 GLIN N30256 FSN 6625-066-2525			+			1	
Oscilloscope, Tektronics 581 dc to 85 mc					5	2	
Generator, Signal, SG-511/U GLIN GGϕϕ11 FSN 6625-819-0472				+		3	
Generator, Signal, AN/USM-44 GLIN J53782 FSN 6625-669-4031				+		4	
Generator, Signal, SG-340A/G GLIN GGϕϕ13 FSN 6625-539-9674				+		5	
Generator, Signal, SG-97/FRC GLIN GGϕϕ2ϕ FSN 6625-351-5958				+		6	
Voltmeter, Electronic, AN/USM-98 GLIN Y148ϕϕ FSN 6625-753-2115			+			7	

APPENDIX II

REFERENCES

Following is a list of references available to the operator and organizational repairman of Counter.

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Bulletins, Lubrication Orders, and Modification Work Orders
SB 38-100	Preservation, Packaging, and Packing Materials, Supplies, and Equipment Used by the Army
TM-38-750	The Army Equipment Records System and Procedures
TM-11-690	Basic Transistor Theory and Applications of Transistors

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The Metric System and Equivalents

Linear Measure

1 centimeter = 10 millimeters = .39 inch
1 decimeter = 10 centimeters = 3.94 inches
1 meter = 10 decimeters = 39.37 inches
1 dekameter = 10 meters = 32.8 feet
1 hectometer = 10 dekameters = 328.08 feet
1 kilometer = 10 hectometers = 3,280.8 feet

Weights

1 centigram = 10 milligrams = .15 grain
1 decigram = 10 centigrams = 1.54 grains
1 gram = 10 decigram = .035 ounce
1 decagram = 10 grams = .35 ounce
1 hectogram = 10 decagrams = 3.52 ounces
1 kilogram = 10 hectograms = 2.2 pounds
1 quintal = 100 kilograms = 220.46 pounds
1 metric ton = 10 quintals = 1.1 short tons

Liquid Measure

1 centiliter = 10 milliters = .34 fl. ounce
1 deciliter = 10 centiliters = 3.38 fl. ounces
1 liter = 10 deciliters = 33.81 fl. ounces
1 dekaliter = 10 liters = 2.64 gallons
1 hectoliter = 10 dekaliters = 26.42 gallons
1 kiloliter = 10 hectoliters = 264.18 gallons

Square Measure

1 sq. centimeter = 100 sq. millimeters = .155 sq. inch
1 sq. decimeter = 100 sq. centimeters = 15.5 sq. inches
1 sq. meter (centare) = 100 sq. decimeters = 10.76 sq. feet
1 sq. dekameter (are) = 100 sq. meters = 1,076.4 sq. feet
1 sq. hectometer (hectare) = 100 sq. dekameters = 2.47 acres
1 sq. kilometer = 100 sq. hectometers = .386 sq. mile

Cubic Measure

1 cu. centimeter = 1000 cu. millimeters = .06 cu. inch
1 cu. decimeter = 1000 cu. centimeters = 61.02 cu. inches
1 cu. meter = 1000 cu. decimeters = 35.31 cu. feet

Approximate Conversion Factors

To change	*To*	*Multiply by*	*To change*	*To*	*Multiply by*
inches	centimeters	2.540	ounce-inches	Newton-meters	.007062
feet	meters	.305	centimeters	inches	.394
yards	meters	.914	meters	feet	3.280
miles	kilometers	1.609	meters	yards	1.094
square inches	square centimeters	6.451	kilometers	miles	.621
square feet	square meters	.093	square centimeters	square inches	.155
square yards	square meters	.836	square meters	square feet	10.764
square miles	square kilometers	2.590	square meters	square yards	1.196
acres	square hectometers	.405	square kilometers	square miles	.386
cubic feet	cubic meters	.028	square hectometers	acres	2.471
cubic yards	cubic meters	.765	cubic meters	cubic feet	35.315
fluid ounces	milliliters	29,573	cubic meters	cubic yards	1.308
pints	liters	.473	milliliters	fluid ounces	.034
quarts	liters	.946	liters	pints	2.113
gallons	liters	3.785	liters	quarts	1.057
ounces	grams	28.349	liters	gallons	.264
pounds	kilograms	.454	grams	ounces	.035
short tons	metric tons	.907	kilograms	pounds	2.205
pound-feet	Newton-meters	1.356	metric tons	short tons	1.102
pound-inches	Newton-meters	.11296			

Temperature (Exact)

°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

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